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1. INTRODUCTION

17MB130 main board is driven by MStar SOC. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU.

This board can be driven just 50Hz UHD panels.

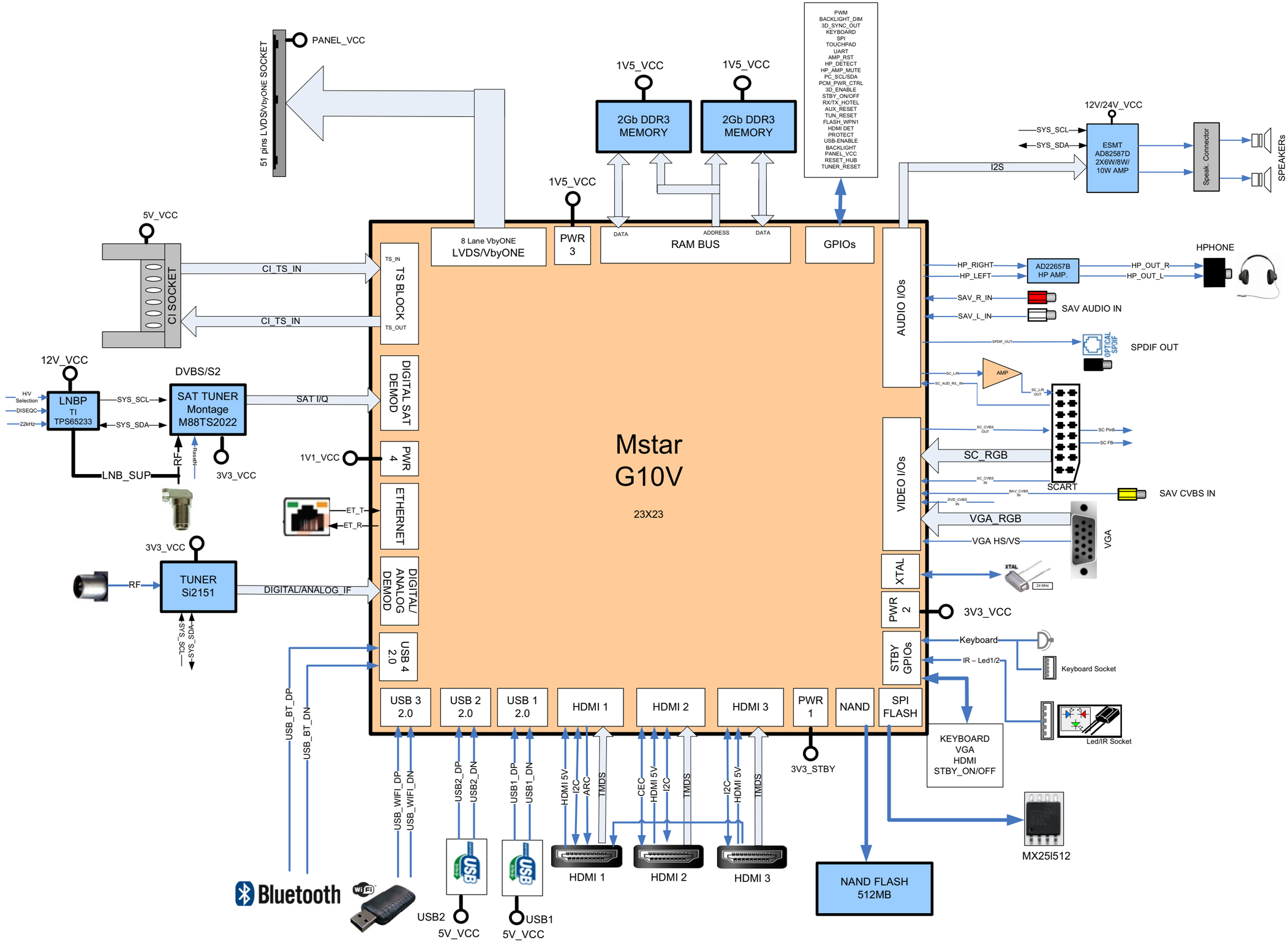
Key features include:

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- The MACEpro video processor
- Home theatre sound processor
- Rich internet connectivity and completed digital home network solution
- Dual-stream decoder for 3D contents
- Mılti-purpose CPU for OS and multimedia
- Peripheral and power management
- Embedded DRAM (for connected option)

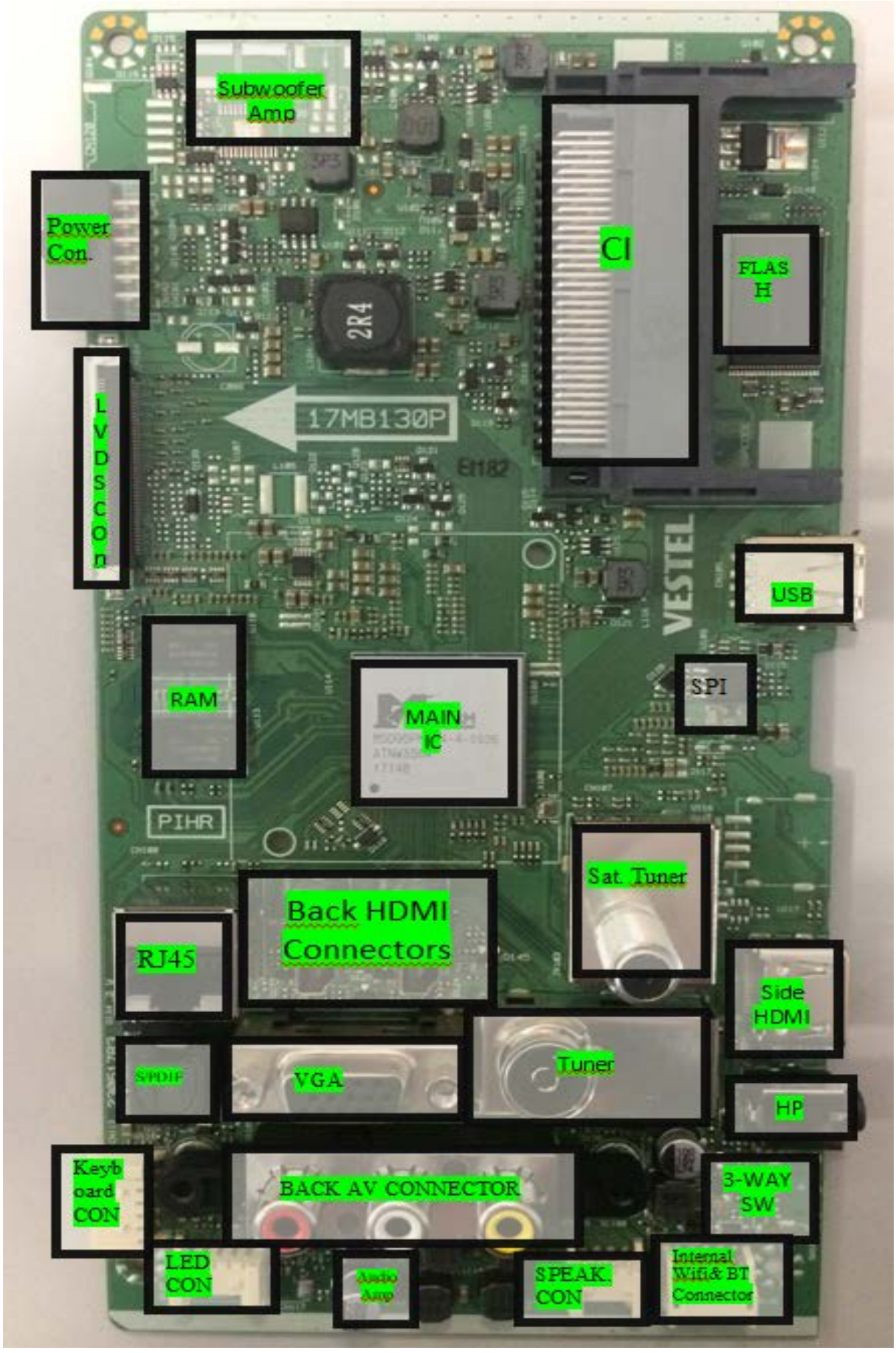
Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Back AV (CVBS, R/L_Audio)
- 1 YPbPr (from VGA with special cable) (Optional)
- 1 PC input(Common)
- 2xBack HDMI 1x Side HDMI input (with ARC option from 2nd input)
- 1 Common interface(Common)
- 1 Optic/ Quax S/PDIF output
- 1 Headphone(Common)
- 2 USB(1X Side Common, 1X Side Optional) and 2x internal USB for Wifi/Bluetooth
- 1 Ethernet-RJ45
- 1 3way/External Touchpad/Tact Switch (Common)

A. GENERAL BLOCK DIAGRAM



B. PLACEMENT OF BLOCKS



2. T/T2/C/A TUNER (U118)

Description:

The Si2151 is Silicon Labs' sixth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wirewound inductors or LNAs, the Si2151 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2151 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners. The Si2151 offers increased immunity to WiFi and LTE interference, eliminating the need for external filtering. For the best performance with next-generation digital TV standards, such as DVB-T2/C2, the Si2151 delivers industry-leading phase noise performance.

Features:

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVBT2/T/C2/C, ISDB-T/C, DTMB
- 1.7 MHz, 6 MHz, 7 MHz, 8 MHz, and 10 MHz channel bandwidths
- 42-1002 MHz frequency range
- Industry-leading margin to A/74, NorDig, DTG, ARIB, EN55020, OpenCable™,DTMB
- Lowest BOM for a hybrid TV tuner
  - No balun, SAW filters, or external inductors required
  - Increased ESD protection on 4pins
- Best-in-class real-world reception
  - Lowest phase noise
  - High Wi-Fi and LTE immunity
- Low power consumption
  - 3.3 V and 1.8 V power supplies
  - Integrated 1.8 V LDO for 3.3 V singlesupply operation
- Integrated power-on reset circuit
- Standard CMOS process
- 3x3 mm, 24-pin QFN package
- RoHS compliant

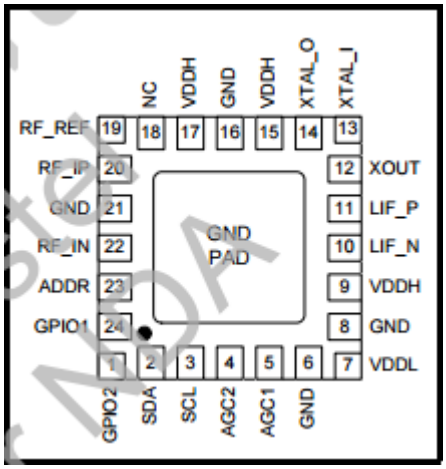


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Figure 1.1 Si2151 Pin description

Pin Number(s)	Name	I/O	Description
1*	GPIO2	I/O	General purpose input/output #1
2	SDA	I/O	I^2C data input/output
3	SCL	I	I^2C clock input
4*	AGC2	I	LIF output amplitude control input #2
5*	AGC1	I	LIF output amplitude control input #1
6	GND	S	Ground
7	VDDL	S	Low supply voltage, 1.8 V (leave caps connected for single supply case)
8	GND	S	Ground
9	VDDH	S	High supply voltage, 3.3 V
10	LIF_N	O	Negative LIF differential output to SoC or DTV/ATV demodulator
11*	LIF_P	O	Positive LIF differential output to SoC or DTV/ATV demodulator
12	XOUT	O	Output reference clock to secondary tuner or receiver
13	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)
14	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)
15	VDDH	S	High supply voltage, 3.3 V
16	GND	S	Ground

17	VDDH	S	High supply voltage, 3.3 V
18*	NC	NC	No connect
19	RF_REF	O	RF reference voltage output
20	RF_IP	I	RF input (positive)
21	GND	S	Ground
22	RF_IN	I	RF input (negative)
23	ADDR	I	I^2C address select
24*	GPIO1	I/O	General purpose input/output #1
***Note:** Pin should be left floating if unused.			

3. S/S2 TUNER (U116) OPTIONAL

Description

The M88TS2022 is a single-chip, direct-conversion tuner for digital satellite receiver applications. It offers the industry's most integrated solution to a satellite tuner function, simplifying the front-end designs. The device also provides an RF bypass output for driving a second tuner module.

This device incorporates the following functional blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with an integrated auxiliary clock output.

As a result of integrating all these blocks, the M88TS2022 has the least number of pins compared with other conventional solutions, and requires the least external components. In typical applications, the M88TS2022 requires only one crystal, one bypass capacitor, one matching network, and a few external resistors. The device also has the industry's smallest latency, as it uses a fast locking PLL and a fast settling DC offset cancellation architecture.

The M88TS2022 can be configured via a 2-wire serial bus. The chip is available in a 28-pin QFN package.

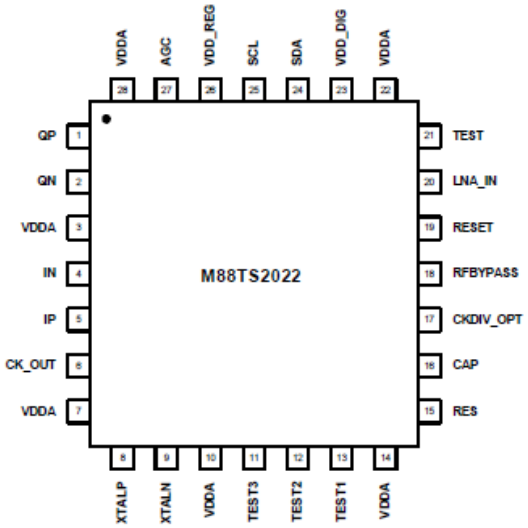
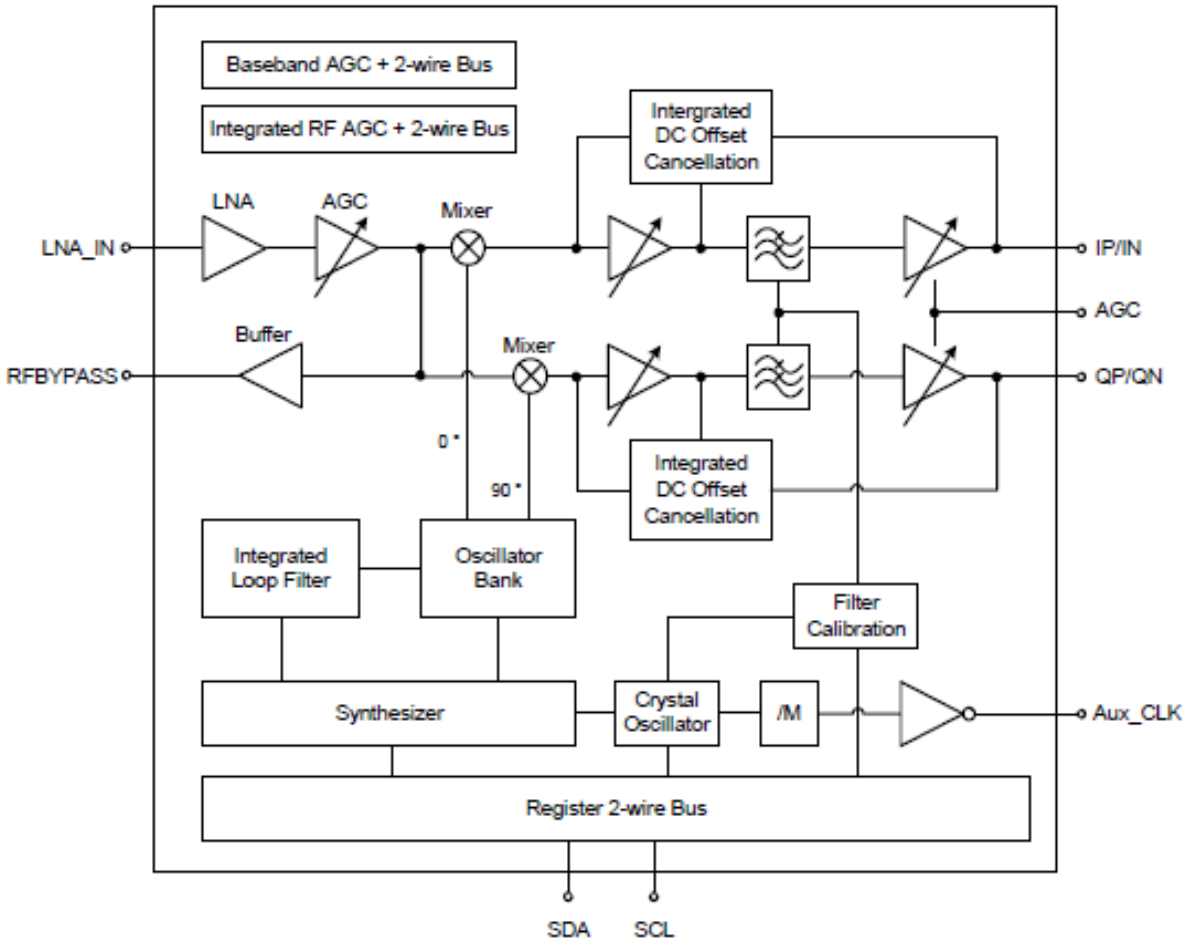


Figure: Pin description

Features

- Single-Chip tuner
- Compliant with DVB-S2 and ABS-S standards
- Support PSK, (PSK and 16APSK
- Direct-conversion from L-band to baseband
- Symbol rate:1 to 45 Msybol/s
- Integrated VCOs and PLL, with on-chip inductors varactors and loop filter
- Integrated RF AGC for optimal performance
- Integrated baseband DC offset cancellation removes external loop filters
- Excellent immunity to strong adjacent undersired channels
- Integrated clock driver provides auxiliary divided clock output for other devices
- Selectable RF bypass
- Support sleep mode
- 2-wire serial bus with 3.3V compatible logic levels
- Power supply+3.3V
- 28-pin QFN package
- RoSH compliant

Block Diagram



4. AUDIO AMPLIFIER STAGES

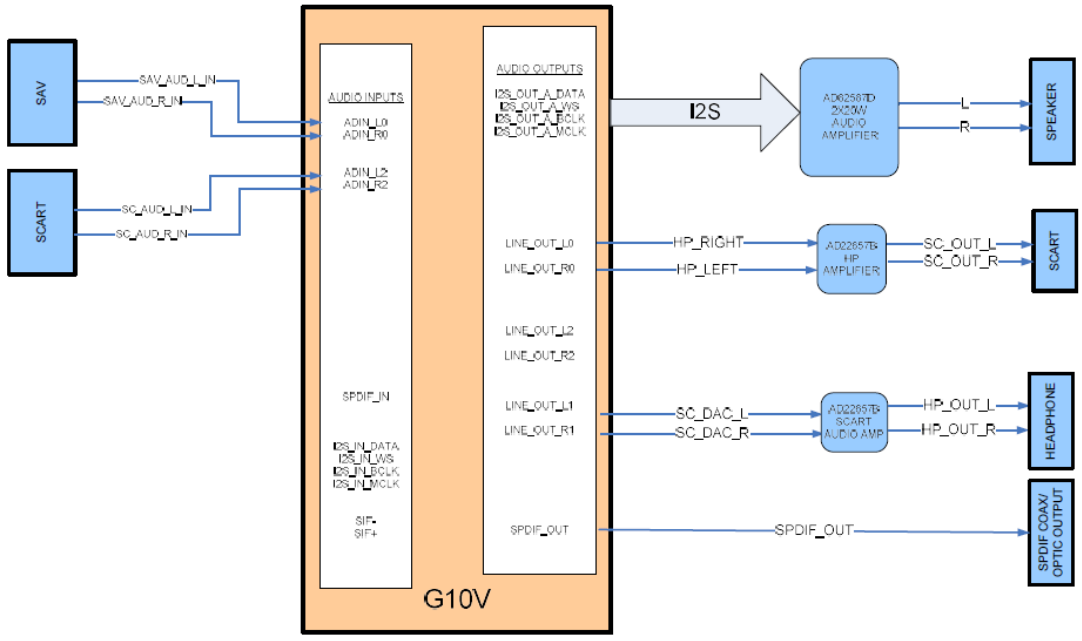


Figure: The block diagram of the audio part

A. *MAIN AMPLIFIER (U123) (8W/10W/12W OPTIONS)*

Description

AD82587D is a digital audio amplifier capable of driving a pair of 8 ohm, 20W or a single 4 ohm, 40W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I^2C digital control interface, the user can control AD82587D's input format selection, DRC (dynamic range control), mute and volume control functions. AD82587D has many built-in protection circuits to safeguard AD82587D from connection errors.

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting) Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  - 32kHz / 44.1kHz / 48kHz and
  - 64kHz / 88.2kHz / 96kHz and
  - 128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x,1024x Fs
  - 256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  - 128x~512x Fs for 64kHz / 88.2kHz / 96kHz

  - 64x~256x Fs for 128kHz /176.4kHz/192kHz

- Supply voltage
  - 3.3V for digital circuit
  - 10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
  - 10W x 2ch into 8_ @ 0.16% THD+N
  - 15W x 2ch into 8_ @ 0.18% THD+N
  - 20W x 2ch into 8_ @ 0.24% THD+N
- Loudspeaker output power for Mono@ 24V
  - 20W x 1ch into 4_ @ 0.17% THD+N
  - 30W x 1ch into 4_ @ 0.2% THD+N
  - 40W x 1ch into 4_ @ 0.24% THD+N
- Sounds processing including:
  - Volume control (+24dB~-103dB, 0.125dB/step)
  - Dynamic range control
  - Power clipping
  - Channel mixing
  - User programmed noise gate with hysteresis window
  - DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage
- detection
- Power saving mode
- Dynamic temperature control

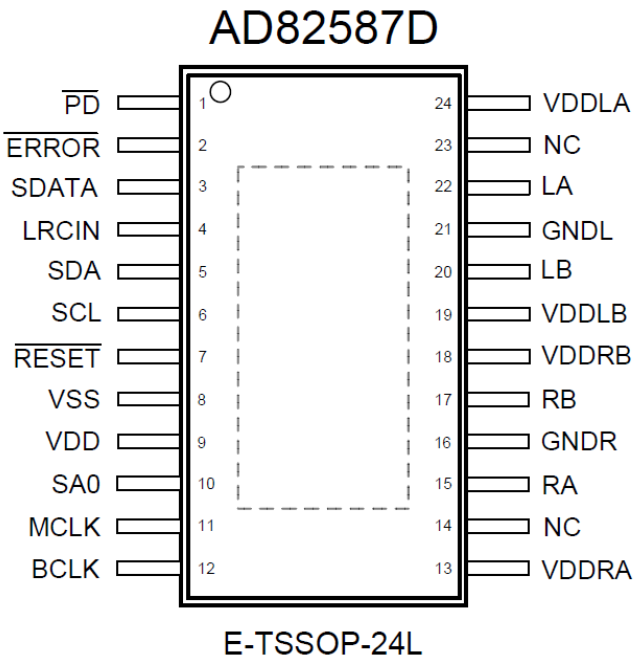


Figure 3.2: Pin description

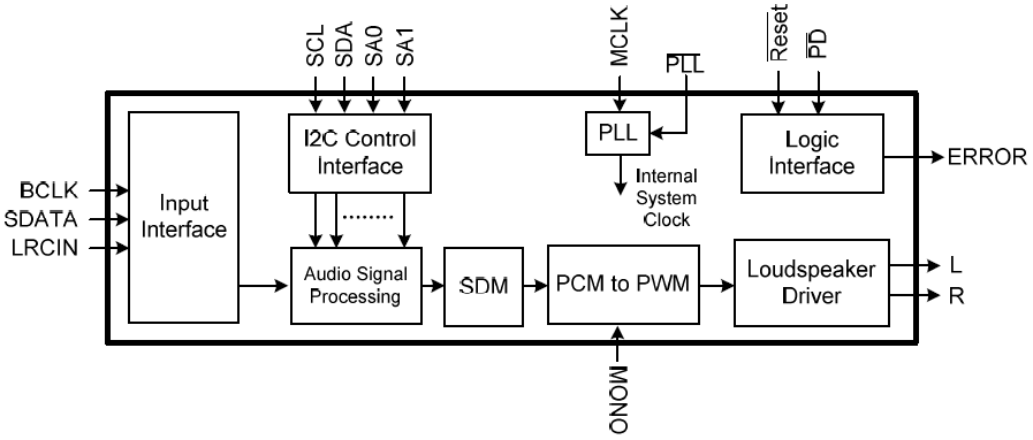


Figure 3.3: Functional Block Diagram

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Table3.1: Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_J	Junction Operating Temperature	0~125	°C
T_A	Ambient Operating Temperature	0~70	°C

Table3.2: Recommended Operating Conditions

B. *HEADPHONE AMPLIFIER (U120)*

Description

The AD22657B is a 2-Vrms cap-less stereo line driver. The device is ideal for single supply electronics. Cap-less design can eliminate output dc-blocking capacitors for better low frequency response and save cost.

The AD22657B is capable of delivering 2-Vrms output into a 10k ohm load with 3.3V supply. The gain settings can be set by users from 1V/V to 10V/V externally. The AD22657B has under voltage protection to prevent POP noise. Build-in shutdown control and de-pop control sequence also help AD22657B to be a pop-less device.

The AD22657B is available in a 10-pin MSOP package.

Features

- Operation Voltage: 3V to 3.6V
- Cap-less Output
  - Eliminates Output Capacitors
  - Improves Low Frequency Response
  - Reduces POP/Clicks
- Low Noise and THD
  - Typical SNR 107dB
  - Typical Vn 7uVrms
  - Typical THD+N < 0.02%
- Maximum Output Voltage Swing into 2.5k Load
  - 2Vrms at 3.3V Supply Voltage
- Single-ended Input
- External Gain Setting from 1V/V to 10V/V
- Fast Start-up Time: 0.5ms
- Integrated De-Pop Control
- External Under Voltage Protection

- Thermal Protection
- Less External Components Required
- +/-8kV IEC ESD Protection at line outputs

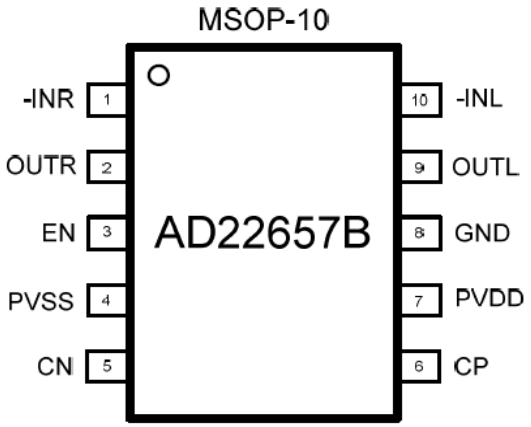


Figure: Pin description

No.	Name	Type (1)	Pin Description
1	-INR	I	Right channel OP negative input
2	OUTR	O	Right channel OP output
3	EN	I	Enable input, active high
4	PVSS	P	Supply voltage
5	CN	I/O	Charge-pump flying capacitor negative terminal
6	CP	I/O	Charge-pump flying capacitor positive terminal
7	PVDD	P	Positive supply
8	GND	P	Ground
9	OUTL	O	Left channel OP output
10	-INL	I	Left channel OP negative input

Table: Pin functions

SYMBOL	PARAMETER		Min	NOM	Max	UNIT
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage	EN		60		% of V_{DD}
V_{IL}	Low Level Input Voltage	EN		40		% of V_{DD}
T_A	Operating Ambient Temperature Range		-40		85	℃
R_L	Load Resistance		600			Ω

Table: Recommended operating conditions

C. SUBWOOFER AMPLIFIER (U126) (12 W)

Description

AD82586C is a digital audio amplifier capable of driving a pair of 8 ohm, 20W operating at 24V supply without external heat-sink or fan requirement with play music.

AD82586C has 20 bands EQ function and can operate 20W stereo or 40W mono optionally.

AD82586C can provide advanced audio processing capabilities, such as volume control, 20 bands speaker EQ, audio mixing, 3D surround and DRC (dynamic range control). These functions are fully programmable via a simple I2C control interface.

Robust protection circuits are provided to protect AD82586C from damage due to accidental erroneous operating condition. AD82586C is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart implemented by analog circuit design. AD82586C is pop free during instantaneous power switch because of its built-in, robust anti-pop circuit.

Features

- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR (A-weighting) Loudspeaker: 99dB (PSNR), 104dB (DR) @24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz / 176.4kHz / 192kHz
- Supply voltage
  3.3V for digital circuit
  10V~26V for loudspeaker driver
- Loudspeaker output power at 24V
  10W x 2CH into 8 ohm @0.17% THD+N for stereo
  20W x 2CH into 8 ohm @0.26% THD+N for stereo
- Sound processing including:
  20 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic Range Control (DRC)
  Dual band DRC

Power clipping

3D surround sound

Channel mixing

Noise gate with hysteresis window

Bass/Treble tone control

DC-blocking high-pass filter

- Anti-pop design
- Short circuit and over-temperature protection
- I^2C control interface with selectable device address
- Support hardware and software reset
- Internal PLL
- LV Under-Voltage shutdown and HV Under-Voltage detection
- Power saving mode

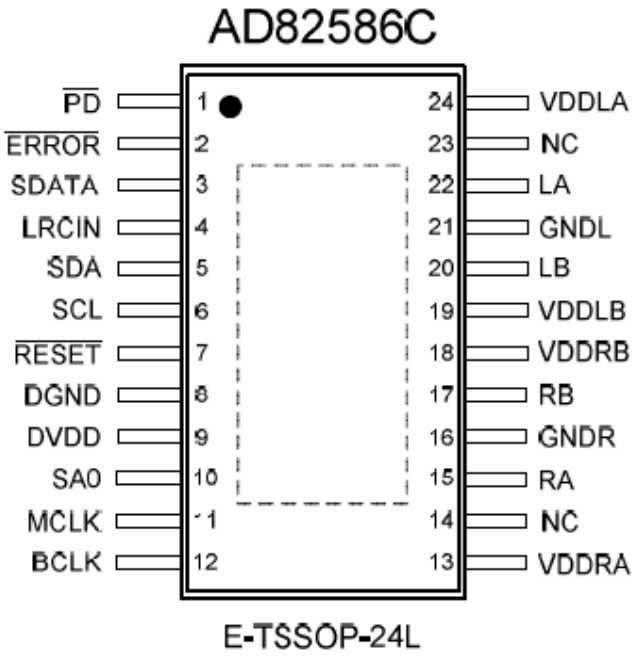


Figure 3.4: Pin description

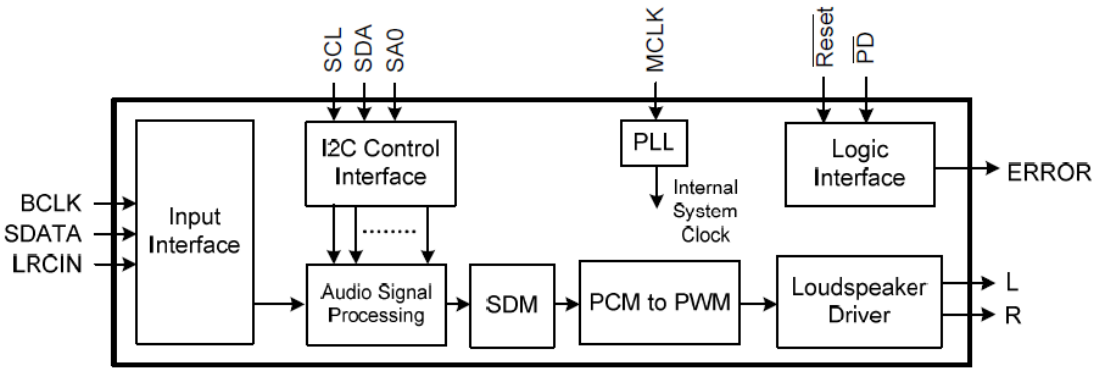


Figure 3.5: Functional Block Diagram

Symbol	Parameter	Min	Max	Units
VDDL/R	Supply for Driver Stage	-0.3	30	V
DVDD	Supply for Digital Circuit	-0.3	3.6	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Table 3.3: Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_A	Ambient Operating Temperature	0~70	°C

Table 3.4: Recommended Operating Conditions

5. POWER STAGE

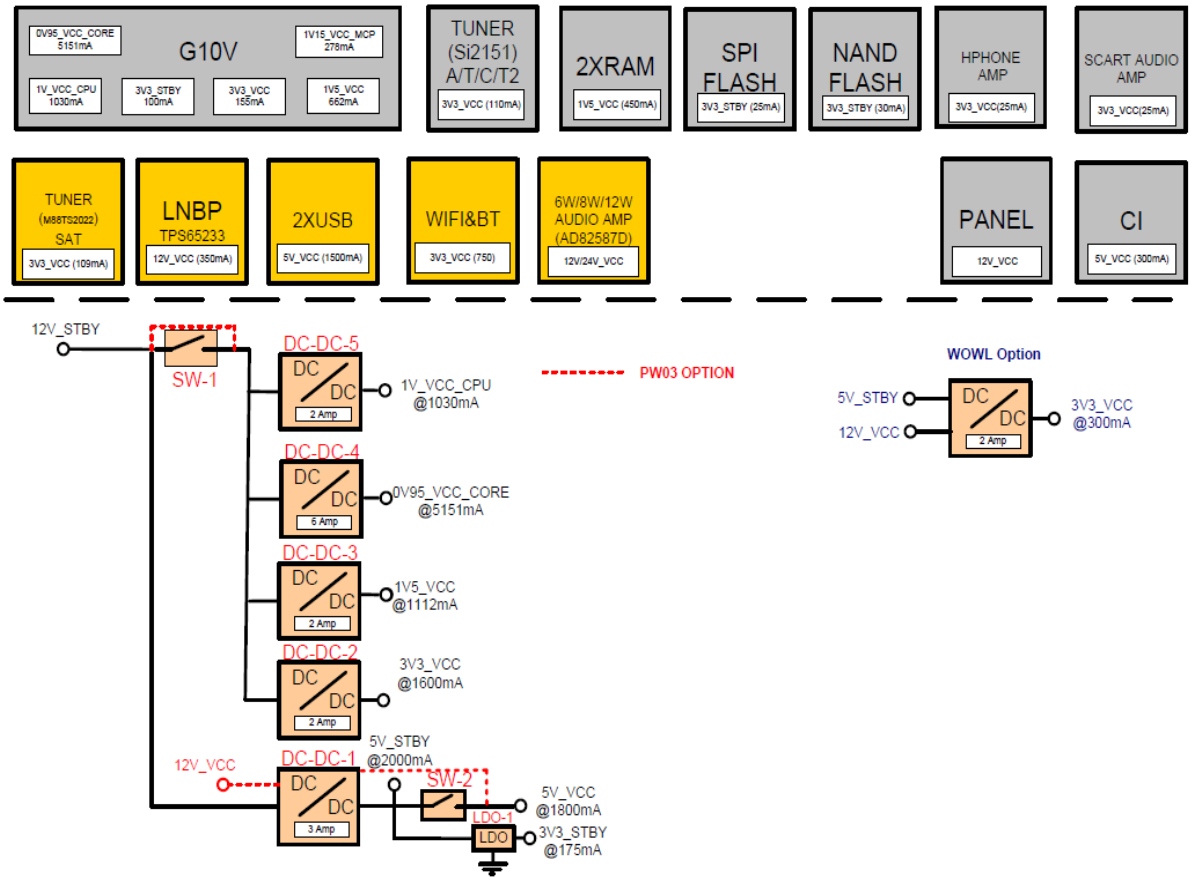


Figure: Power Block Diagram

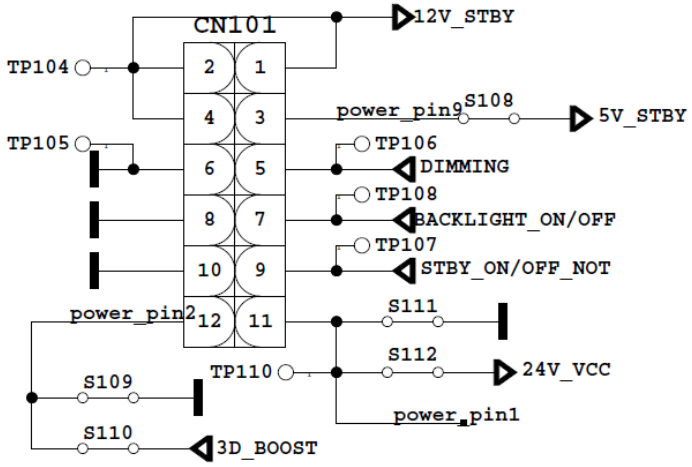


Figure: Power Socket and Power Options

Power socket is used for taking voltages which are 24V_VCC, 12V_STBY and 5V_STBY. These voltages are produced in power card. Also socket is used for giving dimming, backlight and standby signals with power card. Power socket pinning is shown in above figure.

24V_VCC goes directly to the audio part. 12V_STBY is converted several different voltages on the mainboard which are shown in below figure.

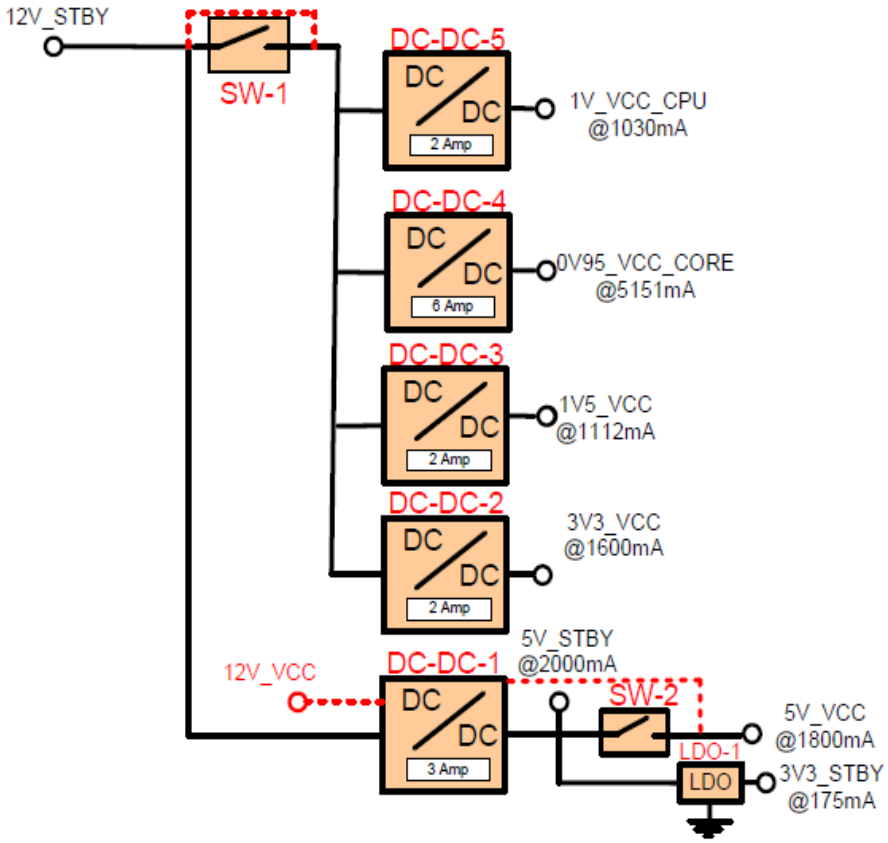


Figure: Power Block Diagram

List of the components:

- SW-1(Q105) → FDC642P
- SW-2(Q100) → NTGS3446
- DC-DC-1(U101) → RT7278G
- DC-DC-2(U100) → TPS563200
- DC-DC-3(U107) → TPS563200
- DC-DC-4(U103) → TPS54821
- DC-DC-5(U104) → TPS563200
- LDO-1(U112) → AP2111H

A. *FDC642P*

Single P-Channel 2.5V Specified PowerTrench® MOSFET
-20 V, -4.0 A, 65 mΩ

Features

- Max $r_{DS(on)}$ = 65 mΩ at V_{GS} = -4.5 V, I_D = -4.0 A
- Max $r_{DS(on)}$ = 100 mΩ at V_{GS} = -2.5 V, I_D = -3.2 A
- Fast switching speed
- Low gate charge (11nC typical)
- High performance trench technology for extremely low $r_{DS(on)}$
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1 mm thick)
- Termination is Lead-free and RoHS Compliant

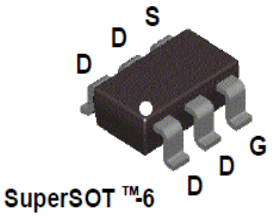
General Description

This P-Channel 2.5V specified MOSFET is produced using Fairchild's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the larger packages are impractical.

Applications

- Load switch
- Battery protection
- Power management



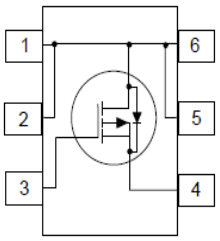


Figure: Pin description

B. *NTGS3446*

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- IDSS Specified at Elevated Temperature
- Pb−Free Package is Available

APPLICATIONS

– Power Management in portable and battery−powered products, i.e. computers, printers, PCMCIA cards, cellular and cordless
– Lithium Ion Battery Applications
– Notebook PC

PIN ASSIGNMENT

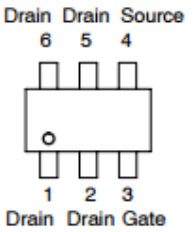


Figure 4.7: Pin description

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	V
Gate–to–Source Voltage	V_{GS}	±12	V
Thermal Resistance Junction–to–Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Drain Current – Continuous @ T_A = 25°C – Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 244 0.5 2.5 10	 °C/W W A A
Thermal Resistance Junction–to–Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Drain Current – Continuous @ T_A = 25°C – Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 128 1.0 3.6 14	 °C/W W A A
Thermal Resistance Junction–to–Ambient (Note 3) Total Power Dissipation @ T_A = 25°C Drain Current – Continuous @ T_A = 25°C – Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 62.5 2.0 5.1 20	 °C/W W A A
Source Current (Body Diode)	I_S	5.1	A
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	°C

Table 4.8: Maximum ratings

C. RT7278G

General Description

The RT7278 is a synchronous DC/DC step-down converter with Advanced Constant On-Time (ACOT™) mode control. It achieves high power density to deliver up to 3A output current from a 4.5V to 18V input supply. The proprietary ACOT™ mode offers an optimal transient response over a wide range of loads and all kinds of ceramic capacitors, which allows the device to adopt very low ESR output capacitors for ensuring performance stabilization. In addition, RT7278 keeps an excellent constant switching frequency under line and load variation and the integrated synchronous power switches with the ACOT™ mode operation provides high efficiency in whole output current load range. Cycle-by-cycle current limit provides an accurate protection by a valley detection of low side MOSFET and external soft-start setting eliminates input current surge during startup. Protection functions also include output under voltage protection, output over voltage protection, and thermal shutdown.

Features

- **ACOT™ Mode Enables Fast Transient Response**
- **4.5V to 18V Input Voltage Range**
- **3A Output Current**
- **60mΩ Internal Low Site N-MOSFET**
- **Advanced Constant On-Time Control**
- **Support All Ceramic Capacitors**
- **Up to 95% Efficiency**
- **700kHz Switching Frequency**
- **Adjustable Output Voltage from 0.765V to 8V**
- **Adjustable Soft-Start**
- **Cycle-by-Cycle Current Limit**
- **Input Under Voltage Lockout**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

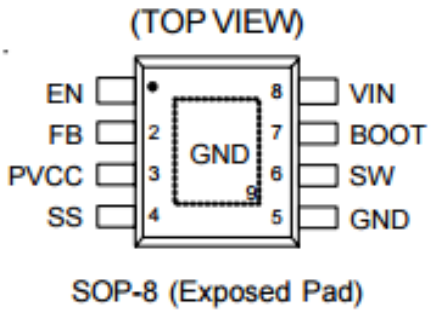


Figure: Pin Assignment

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable Control Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA.
2	FB	Feedback Voltage Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider. The feedback threshold voltage is 0.765V typically.
3	PVCC	Regulator Output for Internal Circuit. Connect a 1μF capacitor to GND to stabilize output voltage.
4	SS	Soft-Start Time Setting. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 3.9nF capacitor sets the soft-start period of V_{OUT} to 2.6ms.
5, 9 (Exposed Pad)	GND	Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.
6	SW	Switch Node. Connect this pin to an external L-C filter.
7	BOOT	Bootstrap Supply for High Side Gate Driver. Connect a 0.1μF or greater ceramic capacitor from BOOT to SW pins.
8	VIN	Power Input. The input voltage range is from 4.5V to 18V. Must bypass with a suitably large (≥10μF x 2) ceramic capacitor.

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	1.5	10	μA
Quiescent Current		I_Q	V_{EN} = 3V, V_{FB} = 1V	--	0.7	--	mA
Logic Threshold							
EN Input Voltage	Logic-High			2	--	18	V
	Logic-Low			--	--	0.4	
V_{FB} Voltage and Discharge Resistance							
Feedback Threshold Voltage		V_{FB}	4.5V ≤ V_{IN} ≤ 18V	0.757	0.765	0.773	V
Feedback Input Current		I_{FB}	V_{FB} = 0.8V	–0.1	0	0.1	μA
V_{PVCC} Output							
V_{PVCC} Output Voltage		V_{PVCC}	6V ≤ V_{IN} ≤ 18V, 0 < I_{PVCC} < 5mA	4.7	5.1	5.5	V
Line Regulation			6V ≤ V_{IN} ≤ 18V, I_{PVCC} = 5mA	--	--	20	mV
Load Regulation			0 < I_{PVCC} < 5mA	--	--	100	mV
Output Current		I_{PVCC}	V_{IN} = 6V, V_{PVCC} = 4V	--	110	--	mA

D. TPS563200

1 Features

- TPS562200 - 2A converter with Integrated 122 mΩ and 72 mΩ FETs
- TPS563200 - 3A converter with Integrated 68 mΩ and 39 mΩ FETs
- D-CAP2™ Mode Control for Fast Transient Response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- 650 kHz Switching Frequency
- Advanced Eco-mode™ Pulse-skip
- Low Shutdown Current Less than 10 µA
- 1% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage
- Cycle-By-Cycle Overcurrent Limit
- Hiccup-Mode Undervoltage Protection
- Non-latch OVP, UVLO and TSD Protections
- Fixed Soft Start: 1 ms

2 Applications

- Digital TV Power Supply
- High Definition Blu-ray Disc™ Players
- Networking Home Terminal
- Digital Set Top Box (STB)

3 Description

The TPS562200 and TPS563200 are simple, easy-to-use, 2 A and 3 A synchronous step-down (buck) converters in 6 pin SOT-23 package.

The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

TPS562200 and TPS563200 operate in Advanced Eco-mode, which maintains high efficiency during light load operation. The devices are available in a 6-pin 1.6mm x 2.9mm SOT (DDC) package, and specified from –40°C to 85°C of ambient temperature.

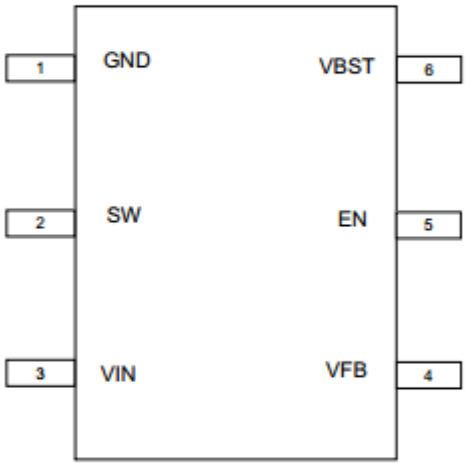


Figure: Pin Assignment

Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect a 0.1µF capacitor between VBST and SW pins.

Electrical Characteristics

T_J = -40°C to 150°C, VIN = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{(VIN)}$	Operating – non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5V, V_{FB} = 0.8 V	TPS562200		230	330	µA
			TPS563200		190	290	
$I_{(VINSDN)}$	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V			3	10	µA
LOGIC THRESHOLD							
$V_{EN(H)}$	EN high-level input voltage	EN		1.6			V
$V_{FN(L)}$	EN low-level input voltage	EN				0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		225	450	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE							
$V_{FB(TH)}$	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, I_O = 10mA, Eco-mode™ operation			772		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode operation		758	765	772	mV
$I_{(VFB)}$	V_{FB} input current	V_{FB} = 0.8V, T_A = 25°C			0	±0.1	µA
MOSFET							
$R_{DS(on)h}$	High side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V	TPS562200		122		mΩ
			TPS563200		68		mΩ
$R_{DS(on)l}$	Low side switch resistance	T_A = 25°C	TPS562200		72		mΩ
			TPS563200		39		mΩ
CURRENT LIMIT							
I_{ocl}	Current limit (1)	DC current, V_{OUT} = 1.05 V, L_{OUT} = 2.2 µF	TPS562200	2.5	3.2	4.3	A
		DC current, V_{OUT} = 1.05 V, L_{OUT} = 1.5 µF	TPS563200	3.5	4.2	5.3	A
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold (1)	Shutdown temperature			155		°C
		Hysteresis			35		
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
V_{OVP}	Output OVP threshold	OVP Detect			125% x Vfbth		
V_{UVP}	Output Hiccup threshold	Hiccup detect			65% x Vfbth		
$t_{HiccupOn}$	Hiccup On Time	Relative to soft-start time			1		ms
$t_{HiccupOff}$	Hiccup Off Time	Relative to soft-start time			7		ms
UVLO							
UVLO	UVLO threshold	Wake up VIN voltage		3.45	3.75	4.05	V
		Hysteresis VIN voltage		0.13	0.32	0.55	

(1) Not production tested

E. TPS54821

General Description

The TPS54821 in thermally enhanced 3.5 mm x 3.5 mm QFN package is a full featured 17 V, 8 A synchronous step down converter which is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. Further space savings are achieved through current mode control, which reduces component count, and by selecting a high switching frequency, reducing the inductor's footprint. The output voltage startup ramp is controlled by the SS/TR pin which allows operation as either a stand alone power supply or in tracking situations. Power sequencing is also possible by correctly configuring the enable and the open drain power good pins. Cycle by cycle current limiting on the high-side FET protects the device in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit which turns off the low-side MOSFET to prevent excessive reverse current. Hiccup protection will be triggered if the overcurrent condition has persisted for longer than the preset time. Thermal hiccup protection disables the device when the die temperature exceeds the thermal shutdown temperature and enables the part again after the built-in thermal shutdown hiccup time.

Features

- Integrated 26 mΩ / 19 mΩ MOSFETs
- Split Power Rail: 1.6 V to 17 V on PVIN
- 200 kHz to 1.6 MHz Switching Frequency
- Synchronizes to External Clock
- 0.6V ±1% Voltage Reference Over Temperature
- Low 2 μA Shutdown Quiescent Current
- Monotonic Start-Up into Pre-biased Outputs
- –40°C to 125°C Operating Junction Temperature Range
- Adjustable Input Undervoltage Lockout
- Adjustable Slow Start/Power Sequencing
- Power Good Output Monitor for Undervoltage and Overvoltage
- Adjustable Input Undervoltage Lockout

APPLICATIONS

- Digital TV Power Supplies
- Set Top Boxes
- Blu-ray DVDs
- Home Terminals

		VALUE		UNIT
		MIN	MAX	
Input Voltage	VIN	–0.3	20	V
	PVIN	–0.3	20	
	EN	–0.3	6	
	BOOT	–0.3	27	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	6	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	6	
Output Voltage	BOOT-PH	0	7.5	V
	PH	–1	20	
	PH 10ns Transient	–3	20	
Vdiff (GND to exposed thermal pad)		–0.2	0.2	V
Source Current	RT/CLK		±100	µA
	PH		Current Limit	A
Sink Current	PH		Current Limit	A
	PVIN		Current Limit	
	COMP		±200	µA
	PWRGD	–0.1	5	mA
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)			2	kV
Electrostatic Discharge (CDM) QSS 009-147 (JESD22-C101B.01)			500	V
Operating Junction Temperature		–40	125	°C
Storage Temperature		–65	150	

Table 4.5: Recommended operating conditions

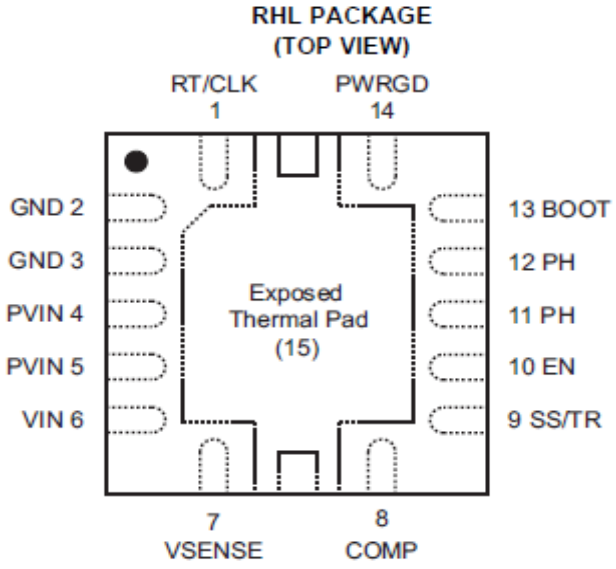


Figure 4.5 : Pin Description

PIN		DESCRIPTION
NAME	NO.	
RT/CLK	1	Automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device; In CLK mode, the device synchronizes to an external clock.
GND	2, 3	Return for control circuitry and low-side power MOSFET.
PVIN	4, 5	Power input. Supplies the power switches of the power converter.
VIN	6	Supplies the control circuitry of the power converter.
VSENSE	7	Inverting input of the gm error amplifier.
COMP	8	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
SS/TR	9	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
EN	10	Enable pin. Float to enable. Adjust the input undervoltage lockout with two resistors.
PH	11, 12	The switch node.
BOOT	13	A bootstrap cap is required between BOOT and PH. The voltage on this cap carries the gate drive voltage for the high-side MOSFET.
PWRGD	14	Power Good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage, EN shutdown or during slow start.
Exposed Thermal PAD	15	Thermal pad of the package and signal ground and it must be soldered down for proper operation.

Table 4.6: Pin functions.

F. AP2111

General Description

The AP2111 is CMOS process low dropout linear regulator with enable function, the regulator delivers a guaranteed 600mA (Min) continuous load current. The AP2111 provides 1.2V, 1.8V, 2.5V, 3.3V, 4.8V regulated output and 0.8V to 5V adjustable output, and provides excellent output accuracy 1.5%, it is also provides a excellent load regulation, line regulation and excellent load transient performance due to very fast loop response. The AP2111 has built-in auto discharge function. The AP2111 features low power consumption. The AP2111 is available in SOIC-8, PSOP-8 SOT-223 and SOT-23-5 packages.

Features

- Output Voltage Accuracy: ±1.5%
- Output Current: 600mA (Min)
- Foldback Short Current Protection: 50mA
- Enable Function to Turn On/Off VOUT
- Low Dropout Voltage (3.3V):
- 250mV (Typ) @ IOUT=600mA
- Excellent Load Regulation: 0.2%/A (Typ)
- Excellent Line Regulation: 0.02%/V (Typ)
- Low Quiescent Current: 55μA (Typ)
- Low Standby Current: 0.01μA (Typ)
- Low Output Noise: 50μVRMS
- PSRR: 65dB @ f=1kHz, 65dB @ f=100Hz
- OTSD Protection

- Stable with 1.0µF Flexible Cap: Ceramic, Tantalum and Aluminum Electrolytic
- Operating Temperature Range: -40°C to 85°C
- ESD: MM 400V, HBM 4000V

6. MICROCONTROLLER

A. ***MSTAR G10 MSD95PMVW4 (U114)***

Description

The MSD91QV01 is MStar's latest SOC solution for UHD smart TV. Based on MStar's advanced technologies, the MSD91QV01 is integrated with the high-quality video processor which satisfies a variety of customer's requests for image quality to develop the state-of-the-art DTV system. The CPU delivers high performance for modern Linux. The up-to-date ARM architecture ensures the best software compatibility. Other applications, such as Java, Flash, and so on, are implemented with less efforts.

The MStar Professional PQ Engine includes all of MStar's most advanced color-tuning tools. MStar unique color processor with specially-designed color remapping systems assist System-developers to identify PQ characteristics of all the range of panel models quickly and easily. Moreover, MStar's innovated UltraClear video processor adopts the new technology for multi-frame video recovery so that contents or details can be restored perfectly and the noises or artifacts from broadcasting or internet can be eliminated.

The MSD91QV01 also integrates all-purpose AV decoders for DTV/MM/OTT applications into a single device, reducing the overall system BOM cost. With versatile peripheral connectivity ports, like HDMI, USB, Ethernet, CVBS, SCART, etc., the MSD91QV01 can serve as a high-quality media center in home entertainment field.

The MSD91QV01 also supports legacy multi-standard analog TV standard with adaptive 3D video decoding and VBI data extraction. Similarly the audio decoder is capable of decoding FM, AM, NICAM, A2, BTSC and sound standards.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MSD91QV01 has an ultra-low power standby modecan act upon standby events and wake up the system as required.

Features

MSD91QV01 is a highly integrated UHD DTV solution which supports 8 lanes Vby1, DTV channel decoding, MPEG decoding, , 3D formatter, and security OS. MSD91QV01 can serve full functions of multi-media centers with a high performance AV CODEC/security engines.

Key features includes:

1. *DVB-C/DVB-T/DVB-T2/DVB-S/DVB-S2 Front-End Demodulators*
2. *Advanced ARM CPU*
3. *3D Formatter Engine*
4. *Multi-Standard A/V Format Decoder*
5. *MStar High Performance Video Processor and MStar Professional PQ Engine*
6. *Home Theater Sound Processor*
7. *Peripheral and Power Management*
8. *Robust and Efficient Security Engine*
9. *Full Multi-Media Decoders Including HEVC Decoder Supporting up to UHD/60fps Resolution*

- High Performance Micro-processor
  - ARM Advanced CPU
  - 32KB/32KB I/D cache
  - 256KB L2 cache
  - Supports Neon instruction sets
- Transport Stream De-multiplexer
  - Supports two parallel TS interfaces, with or without sync signal
  - Supports one programmable TS input/output for external CI module
  - Supports external demodulators
  - TS data rate is 120Mbit/s for serial and 24MByte/s for parallel
  - 128 general purpose PID filters and 128 section filters for all transport stream de-multiplexer
  - Supports additional audio/video/PCR filters
  - Supports TS DMA channel for time-shift
  - Supports 3DES/DES and AES encryption/decryption
- MPEG-2 Video Decoder
  - ISO/IEC 11172-2 MPEG-1 video format decoding
  - ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
  - Supports resolution up to HDTV (1080p60, 1080i, 720p) and SDTV
  - Supports dual stream decoding for 3D content
- MPEG-4 Video Decoder
  - ISO/IEC 14496-2 MPEG-4 ASP video decoding up to HD level
  - Supports resolutions up to HDTV (1080p@60fps)
  - Supports DivX Home Theater & HD profiles
  - Supports FLV version1 video format decoding
  - Supports dual stream decoding for 3D content
- H.264 Decoder
  - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 5.0) video decoding
  - Supports resolution up to 4096x2160@30fps
  - Supports bitrate up to 135Mbps, the upper limit of level 5
  - Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
  - Supports SVAF 2ES (for Dual Decode)
  - Supports MVC 3D decoding upto 1080p@60fps
- H.264 MVC Decoder
  - ITU-T H.264, ISO/IEC 14496-10 video decoding (Main and high profile up to level 4.2)
  - Supports resolution up to 1080p@60fps

- HEVC (H.265) Decoder
  - Supports HEVC/H.265 video decoding
  - Supports Main/Main-10 profile, level 5.1, high tier
  - Supports 8-bit/10-bit color depth
  - Supports resolution up to 4096x2160@30fps
  - Supports max bitrate upto 50 Mbps
- Hardware PNG / GIF Decoder
  - Supports up to 8192 x 8192 (per channel 8 bits), or 4096 x 8192(per channel 16 bits) pixel image
  - PNG format 1bpp/2bpp/4bpp/8bpp index(palette) mode support
  - PNG transparency mode support
  - interlaced / non-interlaced GIF support
  - ARGB8888, RGB565, YUV422(YUYV),YUV422(YVYU),gray, gray with alpha output format support
- Hardware JPEG Decoder
  - Supports upto 1920x1080@30fps, 1280x720@60fps
  - Supports formats: 422/411/420/444/422T
  - Supports scaling down ratios: 1/2x1/2, 1/4x1/4, 1/8x1/8
  - Supports both color and grayscale pictures
  - Supports sequential mode, single scan
  - Supports programmable Region of Interest (ROI)
  - Following the file header scan the hardware decoder fully handles the decode process
- VC-1 Video Decoder[Optional]
  - Supports SMPTE-421 (WMV video) decoding up to MH@HL
  - Supports SMPTE-421 (VC1 video) decoding up to AP@L3 (2048x1024p60)
  - Supports dual stream decoding for 3D content
- NTSC/PAL/SECAM Video Decoder
  - Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
  - Automatic standard detection
  - Motion adaptive 3D comb filter
  - Two configurable CVBS & Y/C S-video inputs
  - Supports Teletext, Closed Caption (analog CC 608/ analog CC 708) and V-chip
- Multi-Standard TV Sound Processor
  - Supports BTSC/A2 demodulation
  - Supports NICAM/FM/AM demodulation
  - Supports MTS Mode Mono/Stereo/SAP in BTSC mode
  - Supports Mono/Stereo/Dual in A2/NICAM mode
  - Built-in audio sampling rate conversion (SRC)
  - Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
  - Advanced sound processing options available, for example: Dolby[1], DTS[2]
  - Supports digital audio format decoding:
  - MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3)[Optional], AAC-LC, HE-AAC, WMA, and WMA9 Pro
  - Supports[Optional] Dolby Digital Plus, Dolby Pulse, and MS11/MS12 multistream decoder, including Dolby Digital Encoder for trans-coding streams to Dolby Digital 5.1 (DDCO), DTS M6 multistream decoder/encoder
  - Supports Audio Description
  - Supports MPEG audio encoding
  - Supports time-shifting PVR
  - Supports programmable delay for audio/video synchronization

- Audio Interface
  - Two L/R audio line-inputs
  - Two L/R outputs for main speakers, moniter output, and SCART output
  - Supports stereo headphone driver
  - I2S digital audio output
  - S/PDIF digital audio output and input
  - Support HDMI receiver ARC function
- Analog RGB Compliant Input Ports
  - Three analog ports support up to 1080P
  - Supports PC RGB input up to SXGA@75Hz
  - Supports HDTV RGB/YPbPr/YCbCr
  - Supports Composite Sync and SOG Sync-on-Green
  - Automatic color calibration
- Analogue RGB Auto-Configuration & Detection
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset and gain configuration
  - Sync Detection for H/V Sync
- DVI/HDCP/HDMI Compliant Input Ports
  - Four HDMI/DVI Input port
  - HDMI 2.0b/1.4b Compliant
  - MStar iSwitch for fast HDMI switching
  - HDCP 2.2/1.4 Compliant
  - Embedded HDCP key
  - Support external HDCP 2.2 key
  - Supports HDMI CEC
  - Supports HDMI 3D formats
  - Supports HDMI ARC
  - Robust receiver with excellent long-cable support
- MStar High Performance Video Processor
  - Video Processing Engine
    - Supports up to 4K UHD@60p
    - 10bits/12bits Internal Data Processing
    - Dual-Engine Architecture supporting PIP/PBP
    - Arbitrary Frame Rate Conversion
  - Video Care Technology
    - Video Line Broken Artifact Detection and Removal
    - Video Detection & Repairing Technology for Lousy Inputs such as Internet Streaming
  - Fully Programmable multi-function scaling engine
    - High-Tap Filters with Programmable Parameter
    - An advanced Zoom Algorithm provides Aliasing/Ringing Suppression
    - Nonlinear Video Scaling supports various modes including Panorama
    - Supports Dynamic Scaling for RM, VC-1 **Optional**
    - Fully Programmable Zoom Ratios for Up/Down Scaling
    - Independent Horizontal and Vertical Zoom
  - Deinterlacer
    - Motion Compensated Video Deinterlacing with Motion Object Stabilizer
    - Motion Adaptive Deinterlacer
    - Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal
    - Automatic 3:2/2:2/M:N Pull-Down Detection and Recovery
  - MStar Genuine 3D
    - Supports Mandatory 3D Format
    - 3D Format Auto-Detection
    - Supports 2D to 3D conversion
  - Motion Frame Rate Conversion
    - Supports Frame Repeat Frame Rate Conversion
  - High Dynamic Range
    - Supports SMPTE ST-2084
    - Supports SMPTE ST-2086
    - MStar HDR+ Technology with Standard HDR Ready

Optional **Please see Ordering Guide for details.**

- MStar Professional PQ Engine
  - UltraClear
    - MPEG Artifact Removal
      - ✧ Adaptive Block Noise Reduction
      - ✧ MStar+ Mosquito Noise Cancellation
    - UltraClear Noise Reduction
      - ✧ UltraClear 3D Motion-Estimation Temporal Filtering
    - 3D Noise Reduction
      - ✧ 3D Temporal Noise Reduction for Lousy Air/Cable Input
      - ✧ Cross-Color Suppression Technology
      - ✧ Supports Hanging Dot Search & Removal
  - S-Powers
    - Video Enhancement Processor
      - ✧ MStar+3D Independent Multi-Band Control Sharpness Technology
      - ✧ MStar+ Video Enhancement Algorithm provides Aliasing/Ringing Suppression
      - ✧ Mstar+ Chroma Transient Improvement
      - ✧ Supports Luma Transient Improvement
      - ✧ Real-Time, Content Adaptive Contrast Enhancement with Chroma Compensated
    - Super Resolution
      - ✧ Local Detial Enhancement
      - ✧ Multi-Directional Jagged Compensation Technology
  - MACE
    - MStar Advanced Color Engine
      - ✧ 3D Independent and Accurate Multi-Adaptive Color Manager
      - ✧ Color Stain Removal Technology
    - Standard Color Format and Processing
      - ✧ Fully programmable Input/Ouput CSC
      - ✧ BT601, BT709, BT2020(CL/NCL)
      - ✧ xvYCC601, xvYCC709
      - ✧ AdobeRGB, AdobeYCC601
      - ✧ sRGB, sYCC601
      - ✧ Fully Programmable 12-bits RGB Gamma
    - Gamut Mapping
      - ✧ Nonlinear / Linear RGB Domain Gamut Mapping
      - ✧ Supports 2D Gamut Mapping
      - ✧ The 3rd Generation 3D Gamut Mapping Engine
- Output Interface
  - Single/Dual link 8/10-bit LVDS output
  - 8-lane 8/10-bit Vby1 output (configurable width: 2/4/8 lane)
  - Supports panel resolution up to Full HD 1920x1080@ 60Hz (LVDS 2ch)
  - Supports panel resolution up to Ultra HD @ 60Hz (Vby1 8-lane)
  - Supports dithering options
  - Spread spectrum output frequency for EMI suppression
  - Supports 60Hz 3D polarizd panel (line interleave)
  - Supports Cinema output mode

- CVBS Video Encoder
  - Supports all NTSC/PAL TV Standard
  - Stand-alone scaling engine (no vertical scaling up)
  - Programmable Hue, Contract, Brightness
  - Supports TTX/CC/WSS output
- CVBS Video Output
  - Allows CVBS output of digital content to SCART
- 2D Graphics Engine
  - Hardware Graphics Engine for responsive interactive applications
  - Supports point draw, line draw, rectangle draw/fill and text draw
  - Supports BitBlt, stretch BitBlt, italic Bitblt, Mirror BitBlt and rotate BitBlt
  - Supports alpha-blending operation
  - Supports source/destination color key and alpha key
  - Supports dither
  - Supports color format conversion and format transformation
  - Raster Operation (ROP)
  - Support DFB and Porter-Duff operation
- VIF Demodulator
  - Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards
  - Support low IF architecture
  - Audio/Video internal dual-path processor
  - Locking range improvement
- DVB-C Demodulator
  - Compliant with ITU J.83 Annex A/C DVB-C (EN 300 429)
  - Supports 1-7.2 M Baud symbol rate
  - Automatic blind channel scan (constellation and symbol rate)
  - Supports LIF interfaces
  - IIS performance improvement
- DVB-T Demodulator
  - Compliant with DVB-T (ETSI EN 300 744)
  - Nordig 2.2.2, D-book 7.0 compliant
  - Accept low IF inputs in 6, 7, 8MHz channel bandwidths
  - Supports all guard intervals (1/32 to 1/4)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM)
  - Ultra fast automatic blind UHF/VHF channel scan
  - Optimized for SFN channels with pre/post-cursive echoes inside/outside the guard
  - Phase-Noise suppresion
  - Impulse-Noise suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - CNR performance improvement
  - Outside-GI performance improvement

- DVB-T2 Demodulator
  - Compliant with DVB-T2 (ETSI EN 302 755) v1.3.1, T2-base & T2-Lite profile
  - Nordig Unified 2.2.2, D-Book 7.0 compliant
  - Supports all guard intervals (1/128 to 1/4)
  - Supports all FFT modes from 1K to 32K
  - Supports all long and short block code rates (1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 2/5, 1/3)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM, 256-QAM)
  - Transmit diversity (MISO) support
  - Supports all scattered pilot patterns (PP1 to PP8)
  - Supports rotated and non-rotated constellations
  - Supports single and multiple PLPs
  - Accept low IF inputs in 1.7, 5, 6, 7, 8MHz channel bandwidths
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - Outside GI improvement

- DVB-S Demodulator
  - Compliant with DVB-S (ETSI EN 300 421)
  - Data Rate: 1-70 Msps
  - Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
  - Carrier frequency acquisition range: 5MHz
  - Fast automatic blind scan of symbol rates and carrier frequencies
  - Equalizer compensates for channel impairment
  - DiSEqC™ 2.0 compatible with LNB controller
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Novel carrier recovery algorithms for tracking and compensating large phase noises
  - Integrated FEC decoders for near Shannon limit performances
  - Integrated signal quality and BER monitors
  - Improved CNR performance

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- DVB-S2 Demodulator
  - Compliant with DVB-S2 (ETSI EN 302 307)
  - Data Rate: 1-70 Msps
  - Constellations: QPSK , 8PSK , 16APSK
  - QPSK Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
  - 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10
  - 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
  - Roll-off factors for pulse shaping: 0.2, 0.25, and 0.35
  - Carrier frequency acquisition range: 5MHz
  - Fast automatic blind scan of symbol rates and carrier frequencies
  - Equalizer compensates for channel impairment
  - DiSEqC™ 2.0 compatible with LNB controller
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Novel carrier recovery algorithms for tracking and compensating large phase noises
  - Integrated FEC decoders for near Shannon limit performances
  - Integrated signal quality and BER monitors
- Connectivity
  - Four USB 2.0 host ports
  - USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
  - USB port supports efficient battery charger
  - Embedded Ethernet PHY
- Miscellaneous
  - Supports up to 32-bit DDR3 DRAM
  - Supports PVR
  - Supports Common Interface for conditional access support
  - Bootable SPI interface with serial flash support
  - Parallel NAND flash support
  - Power control module with ultra low power MCU available in standby mode
  - 722-ball BGA package
  - Operating Voltages: 1.5V (DDR3), and 3.3V (I/O and analog)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}	3.14		3.46	V
1.5V Supply Voltages	V_{VDD_15}	1.43		1.57	V
Core Supply Voltages	V_{VDD_core}		TBD		V
CPU Supply Voltages	V_{VDD_cpu}		TBD		V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Table: Recommended operating condition

7. 2GB DDR3 SDRAM

A. ***HYNIX H5TQ2G63GFR-TEC (U113-U110)***

Description

The H5TQ2G63GFR is a 2,147,483,648-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. Hynix 2Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sam-pled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Features

- VDD=VDDQ=1.5V +/- 0.075V
- Fully differential clock inputs (CK, CK) operation
- Differential Data Strobe (DQS, DQS)
- On chip DLL align DQ, DQS and DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 6, 7, 8, 9, 10, 11, 12 and 13 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8, 9, 10
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- Average Refresh Cycle (Tcase 0^oC ~ 95^oC)
    - 7.8 μs at 0^oC ~ 85^oC
    - 3.9 μs at 85^oC ~ 95^oC
- Auto Self Refresh supported Driver strength selected by EMRS
- JEDEC standard 96ball FBGA(x16) Asynchronous RESET pin supported
- Driver strength selected by EMRS TDQS (Termination Data Strobe) supported (x8 only)
- Dynamic On Die Termination supported 8 bit pre-fetch
- Asynchronous RESET pin supported
- ZQ calibration supported
- Write Levelization supported

- On Die Thermal Sensor supported
- 8 bit pre-fetch

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

MEMORY CONFIGURATION OF MB130

	Memory Config				
	SoC Name	**RAM Internal**	**RAM external**	**NAND Flash**	**SPI Flash**
Connected	G10	2X2GBit	2X4Gbit	4Gbit	2MByte
Non-Connected	G10V	NA	2X2Gbit	2Gbit	2MByte

8. 2GBIT - 4GBIT(CONNECTED OPTION) (256M X 8 BIT) NAND FLASH MEMORY

A. *MT29F2G08ABAEAWP (U105)*

Description

Micron NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (I/Ox) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection and monitor device status (R/B#). This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign. A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). There is at least one NAND Flash die per chip enable signal. For further details, see Device and Array Organization. This device has an internal 4-bit ECC that can be enabled using the GET/SET

features or by factory (always enabled). See Internal ECC and Spare Area Mapping for ECC for more information.

Features

- Open NAND Flash Interface (ONFI) 1.0-compliant
- Single-level cell (SLC) technology
- Organization
  - Page size x8: 2112 bytes (2048 + 64 bytes)
  - Page size x16: 1056 words (1024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Plane size: 2 planes x 1024 blocks per plane
  - Device size: 2Gb: 2048 blocks
- Asynchronous I/O performance
  - ^{t}RC/^{t}WC: 20ns (3.3V), 25ns (1.8V)
- Array performance
  - Read page: 25µs
  - Program page: 200µs (TYP: 1.8V, 3.3V
  - Erase block: 700µs (TYP)
- Command set: ONFI NAND Flash Protocol
- Advanced command set
  - Program page cache mode
  - Read page cache mode
  - One-time programmable (OTP) mode
  - Two-plane commands
  - Interleaved die (LUN) operations
  - Read unique ID
  - Block lock (1.8V only)
  - Internal data move
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Ready/Busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: Write protect entire device
- First block (block address 00h) is valid when shipped from factory with ECC. For minimum required ECC, see Error Management.

- Block 0 requires 1-bit ECC if PROGRAM/ERASE cycles are less than 1000
- RESET (FFh) required as first command after poweron
- Alternate method of device initialization (Nand_Init) after power up (contact factory)
- Internal data move operations supported within the plane from which data is read
- Quality and reliability
    - Data retention: 10 years
- Operating voltage range
    - VCC: 2.7–3.6V
    - VCC: 1.7–1.95V
- Operating temperature:
    - Commercial: 0°C to +70°C
    - Industrial (IT): –40ºC to +85ºC
- Package
    - 48-pin TSOP type 1, CPL63-ball VFBGA

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	70	°C
	Industrial		–40	–	85	°C
Vcc supply voltage	1.8V	V_{CC}	1.7	1.8	1.95	V
	3.3V		2.7	3.3	3.6	V
Ground supply voltage		V_{SS}	0	0	0	V

Table: Recommended operating conditions

9. 16M-BIT [16M X 1] CMOS SERIAL FLASH EEPROM

A. KH25L1606EM2-12G MACRONIX SPI FLASH (U115)

Description

The device features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input. When it is in Dual Output read mode, the SI and SO pins become SIO0 and SIO1 pins for data output. The device provides sequential read operation on whole chip. After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page basis, or word basis for erase command is executes on sector, or block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit. Advanced security features enhance the protection and security functions; please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode. The device utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after typical 100,000 programs and erase cycles.

Features

- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 16,777,216 x 1 bit structure or 8,388,608 x 2 bits (Dual Output mode) structure
- 512 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- 32 Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Program Capability
  - Byte base
  - Page base (256 bytes)
- Latch-up protected to 100mA from -1V to Vcc +1V

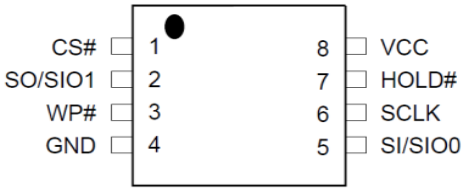
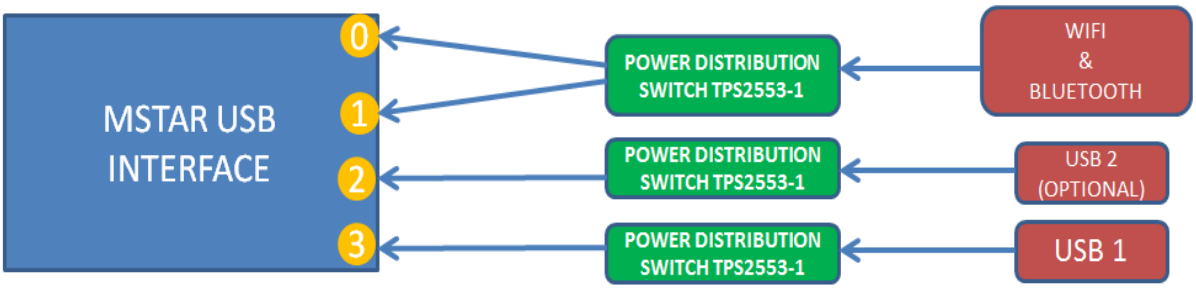


Figure: Pin configuration

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for Dual Output mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Output (for Dual Output mode)
SCLK	Clock Input
WP#	Write protection
HOLD#	Hold, to pause the device without deselecting the device
VCC	+ 3.3V Power Supply
GND	Ground

Table: Pin description

10. USB INTERFACE



A. USB POWER SWITCH TPS2553-1 (U109-U117-U122)

FEATURES

- Up to 1.5 A Maximum Load Current
- ±6% Current-Limit Accuracy at 1.7 A (typ)
- Meets USB Current-Limiting Requirements
- Backwards Compatible with TPS2550/51
- Adjustable Current Limit, 75 mA–1300 mA (typ)
- Constant-Current (TPS2552/53) and Latch-off (TPS2552-1/53-1) Versions
- Fast Overcurrent Response - 2-µs (typ)
- 85-mΩ High-Side MOSFET (DBV Package)
- Reverse Input-Output Voltage Protection
- Operating Range: 2.5 V to 6.5 V
- Built-in Soft-Start
- 15 kV ESD Protection per IEC 61000-4-2 (with External Capacitance)
- UL Listed – File No. E169910 and NEMKO IEC60950-1-am1 ed2.0

APPLICATIONS

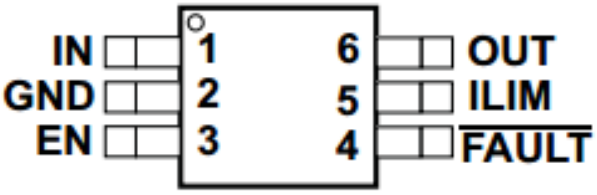
- USB Ports/Hubs
- Digital TV
- Set-Top Boxes
- VOIP Phones

DESCRIPTION

The TPS2552/53 and TPS2552-1/53-1 power-distribution switches are intended for applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered and provide up to 1.5 A of continuous load current. These devices offer a programmable current-limit threshold between 75 mA and 1.7 A (typ) via an external resistor. Current-limit accuracy as tight as ±6% can be achieved at the higher current-limit settings. The power-switch rise and fall times are controlled to minimize current surges during turn on/off.

TPS2552/53 devices limit the output current to a safe level by using a constant-current mode when the output load exceeds the current-limit threshold. TPS2552-1/53-1 devices provide circuit breaker functionality by latching off the power switch during overcurrent or reverse-voltage situations. An internal reverse- voltage comparator disables the power-switch when the output voltage is driven higher than the input to protect devices on the input side of the switch. The $\overline{\text{FAULT}}$ output asserts low during overcurrent and reverse-voltage conditions.

DBV PACKAGE
(TOP VIEW)



EN = Active High for the TPS2553

11. CI INTERFACE

17MB130 Digital CI ve Smart Card Interface Block diagram:

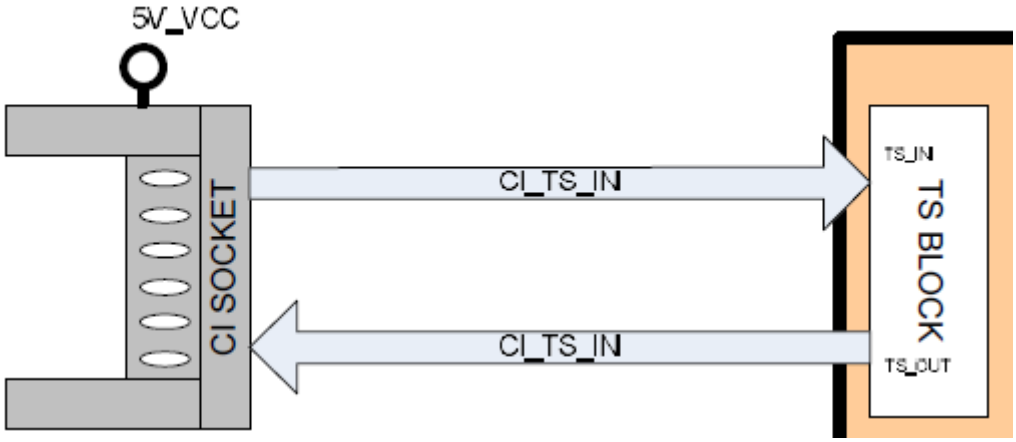


Figure: CI interface

12. SOFTWARE UPDATE

A. ***MAIN SOFTWARE UPDATE***

In MB98 project, please follow software update procedure:

1. mb130_en.bin, mb130_RomBoot.bin, mb130_PM51.bin and usb_auto_update_G10.txt documents should be copied directly inside of a flash memory (not in a folder).
2. Insert flash memory to the TV when TV is powered off.
3. While pushing the OK button in remote control, power on and wait. TV will power-up itself.
4. If First Time Installation screen comes, it means software update procedure is successful.

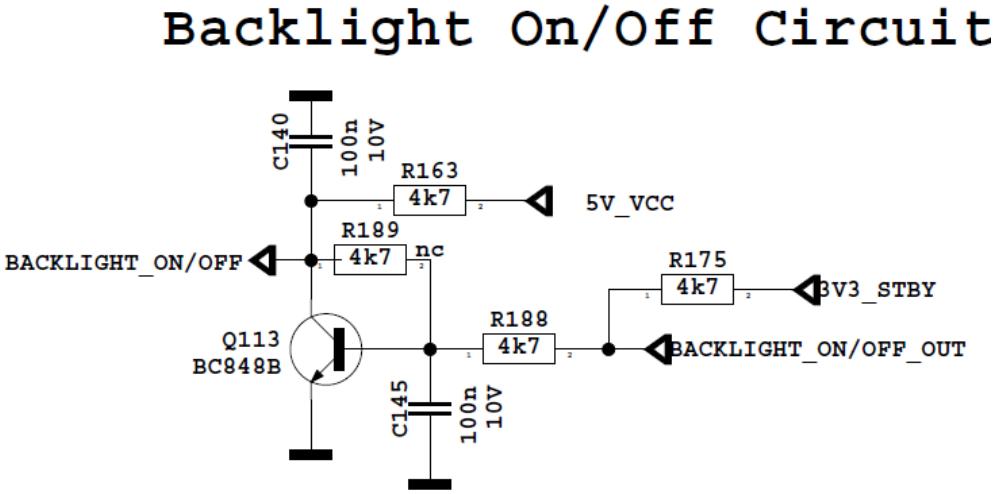
13. TROUBLESHOOTING

A. ***NO BACKLIGHT PROBLEM***

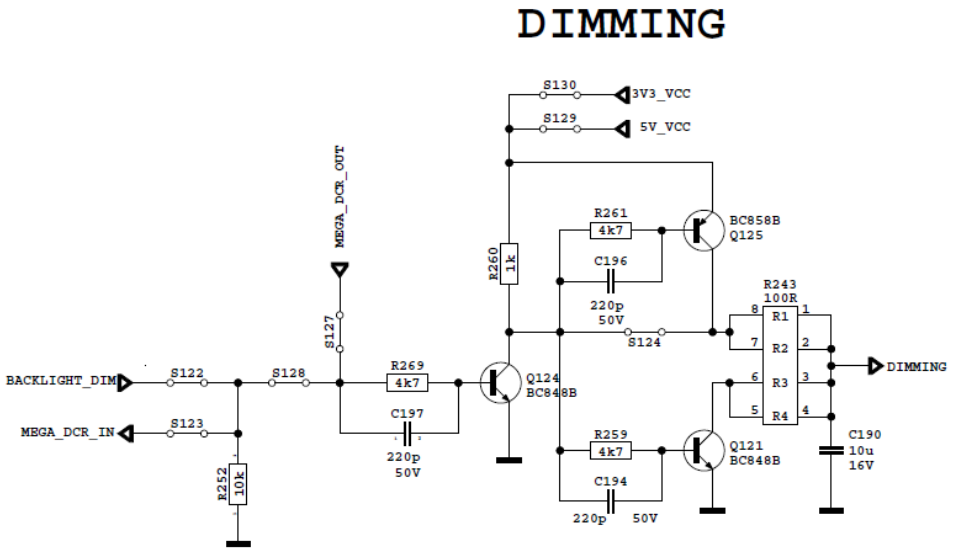
Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply, stby on/off pin

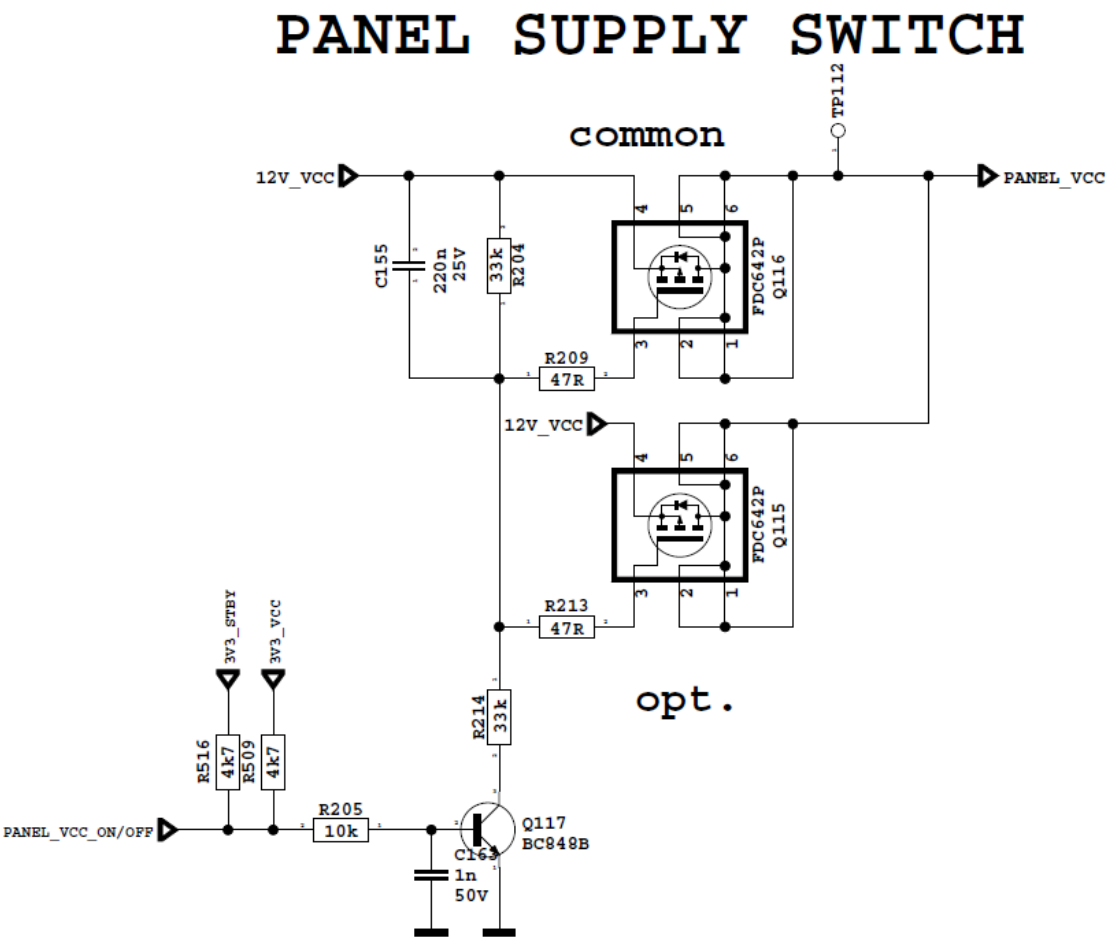
BACKLIGHT_ON/OFF pin should be high when the backlight is ON. Collector pin of Q113 must be low when the backlight is OFF. If it is a problem, please check Q106. Also it can be tested in TP108 in main board. Please also check panel cables.



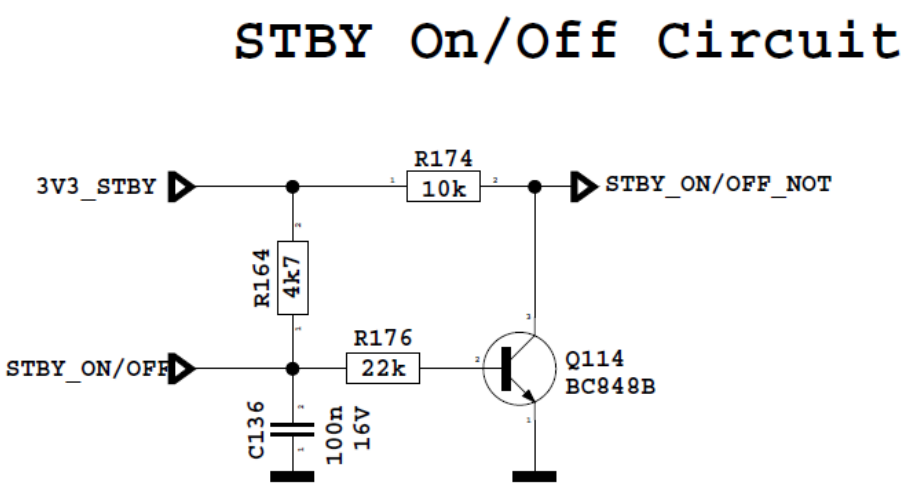
Dimming pin should be high or square wave in open position. If it is low, please check S122 for Mstar side. It also can be checked at TP106. Please also check panel or power cables and connectors.



Backlight power supply should be in panel specs. Please check Q124, shown below; also it can be checked TP112.



STBY_ON/OFF should be low for TV on condition, please check Q114's collector.

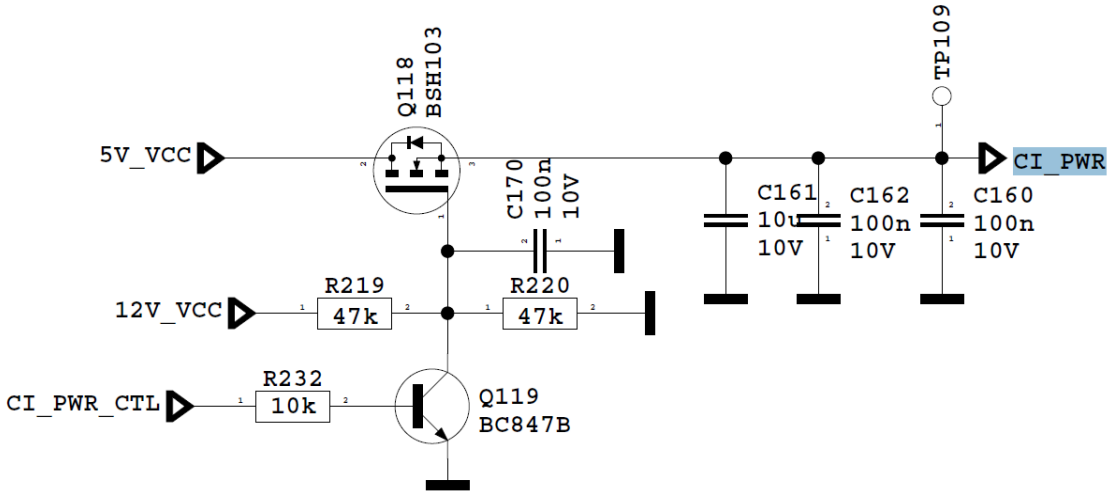


B. CI MODULE PROBLEM

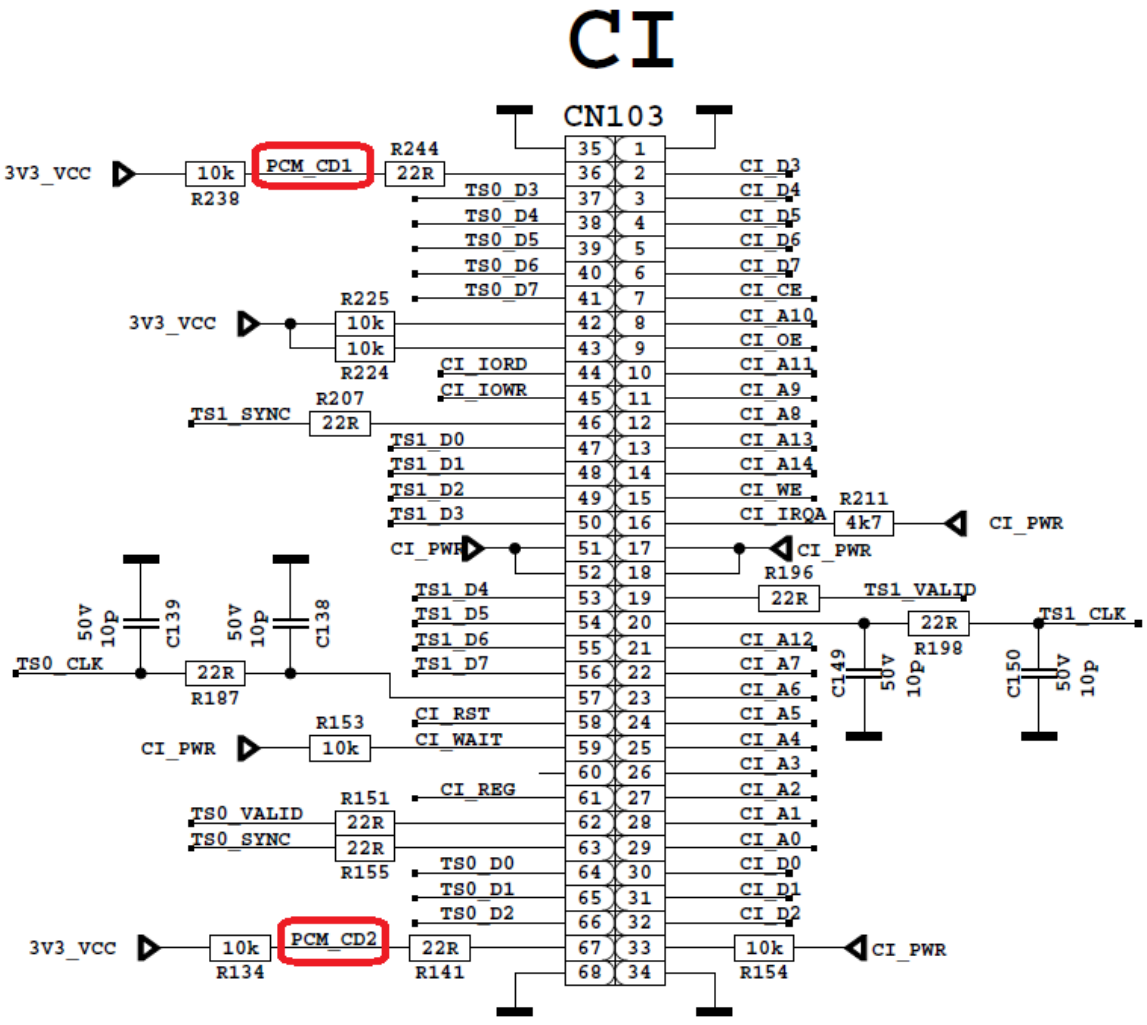
Problem: CI is not working when CI module inserted.

Possible causes: Supply, suply control pin, detects pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTRL, this pin should be low.



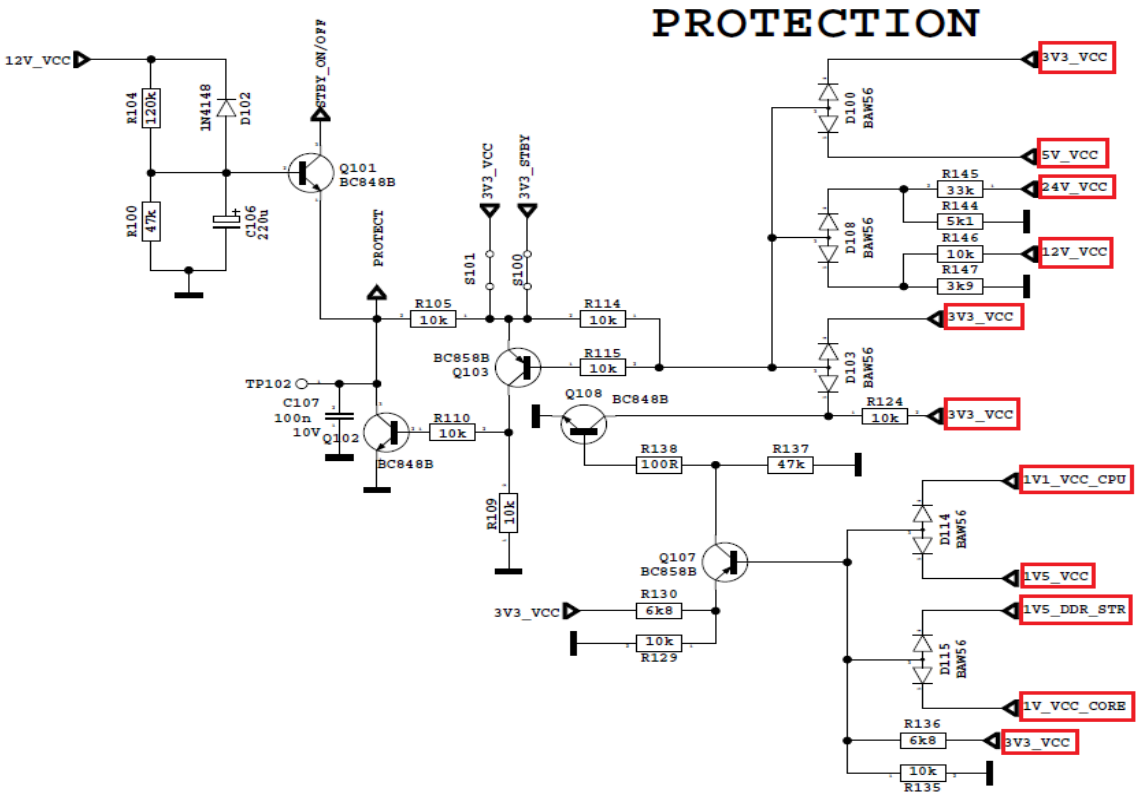
- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.



C. STAYING IN STAND-BY MODE

Problem: Staying in stand-by mode, no other operation.

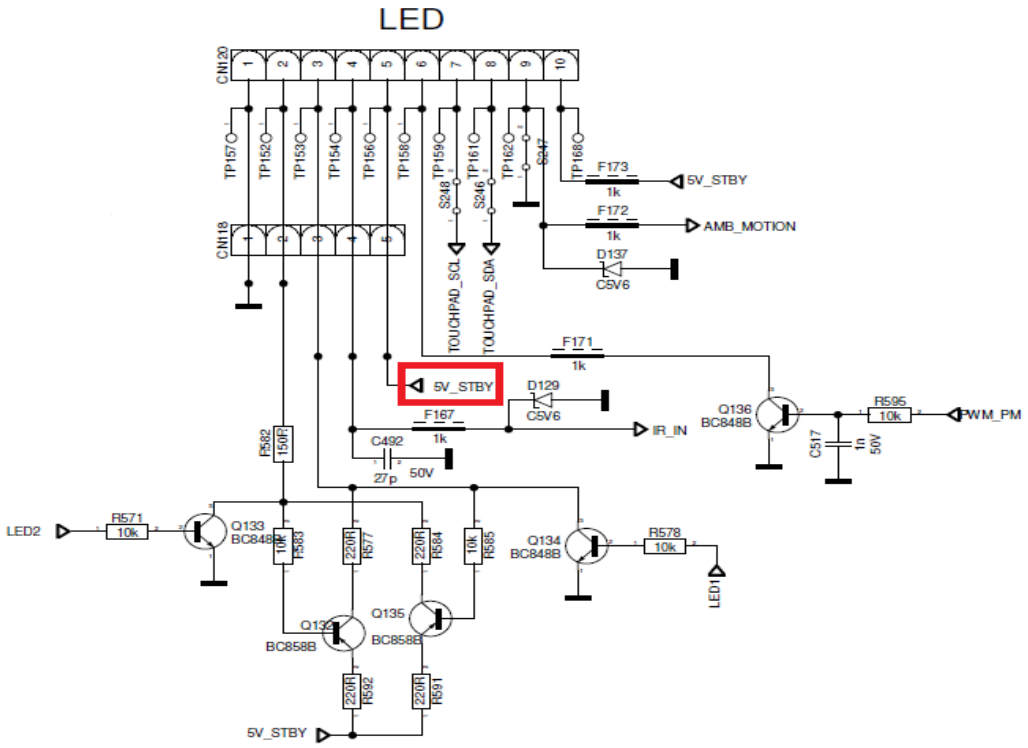
This problem indicates a short on Vcc voltages. Protect pin should be logic high while normal operation. When there is a short circuit protect pin will be logic low. If you detect logic low on protect pin, unplug the TV set and control voltage points with a multimeter to find the shorted voltage to ground.



D. IR PROBLEM

Problem: LED or IR not working

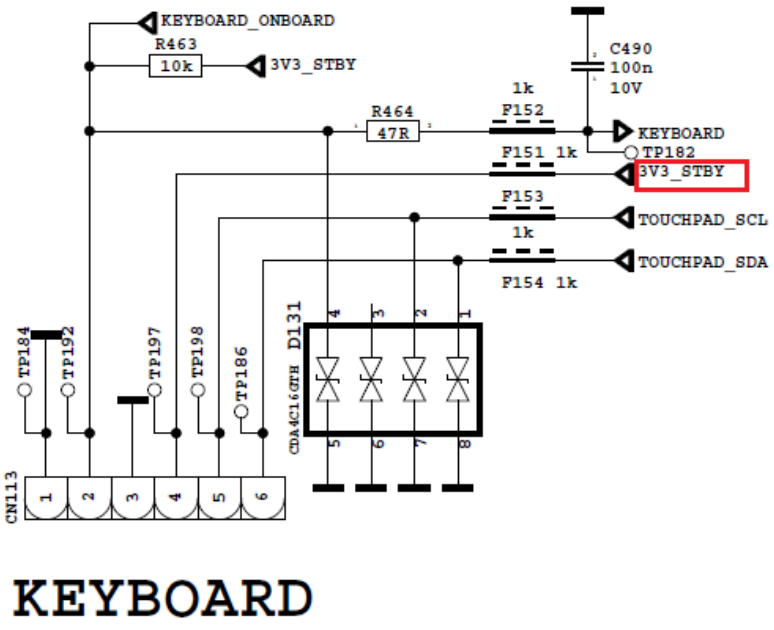
Check LED card supply on MB98 chasis.



E. KEYPAD TOUCHPAD PROBLEMS

Problem: Keypad or Touchpad is not working

Check keypad supply on MB130.

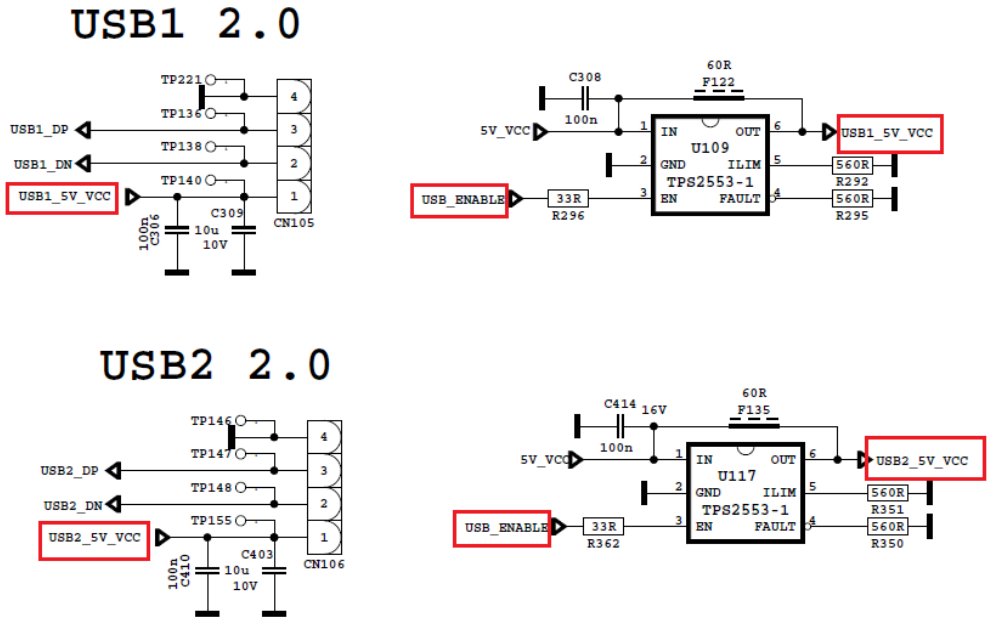


F. USB PROBLEMS

Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

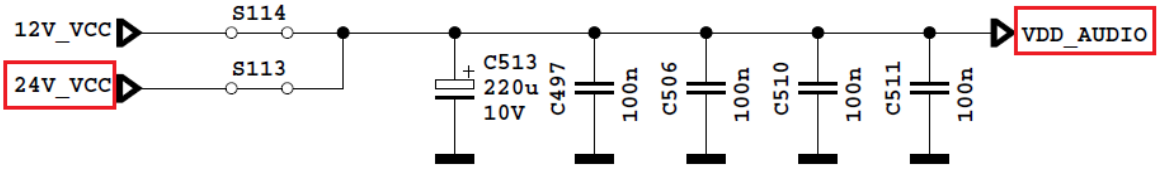
USB Control is optional, so U109 and U117 may not be added. Check supply voltages only.

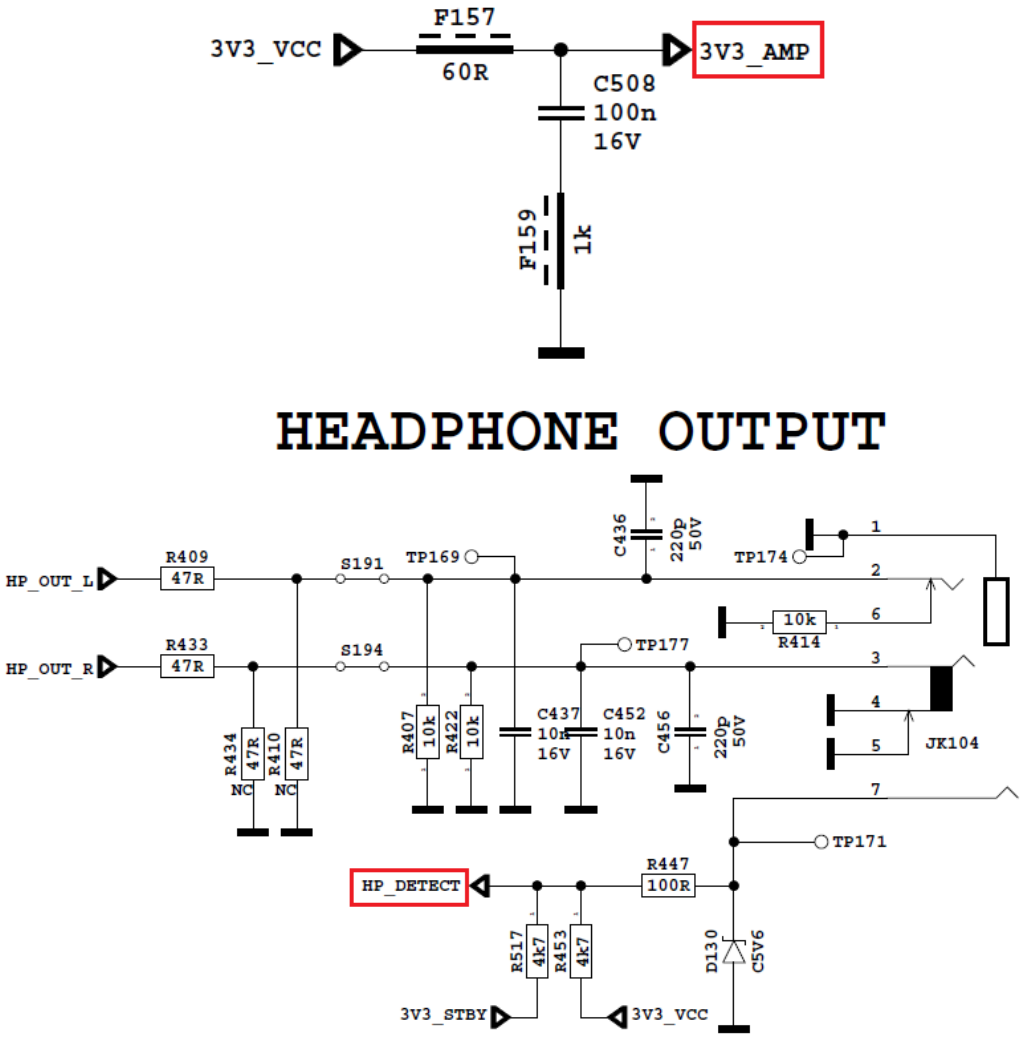


G. NO SOUND PROBLEM

Problem: No audio at main TV speaker outputs.

Check supply voltages of 24V_VCC, VDD_AUDIO and 3V3_AMP with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.





H. STANDBY ON/OFF PROBLEM

Problem: Device cannot boot, TV hangs in standby mode.

There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm program. These printouts may give a clue about the problem. You can use VGA for Teraterm program connection.

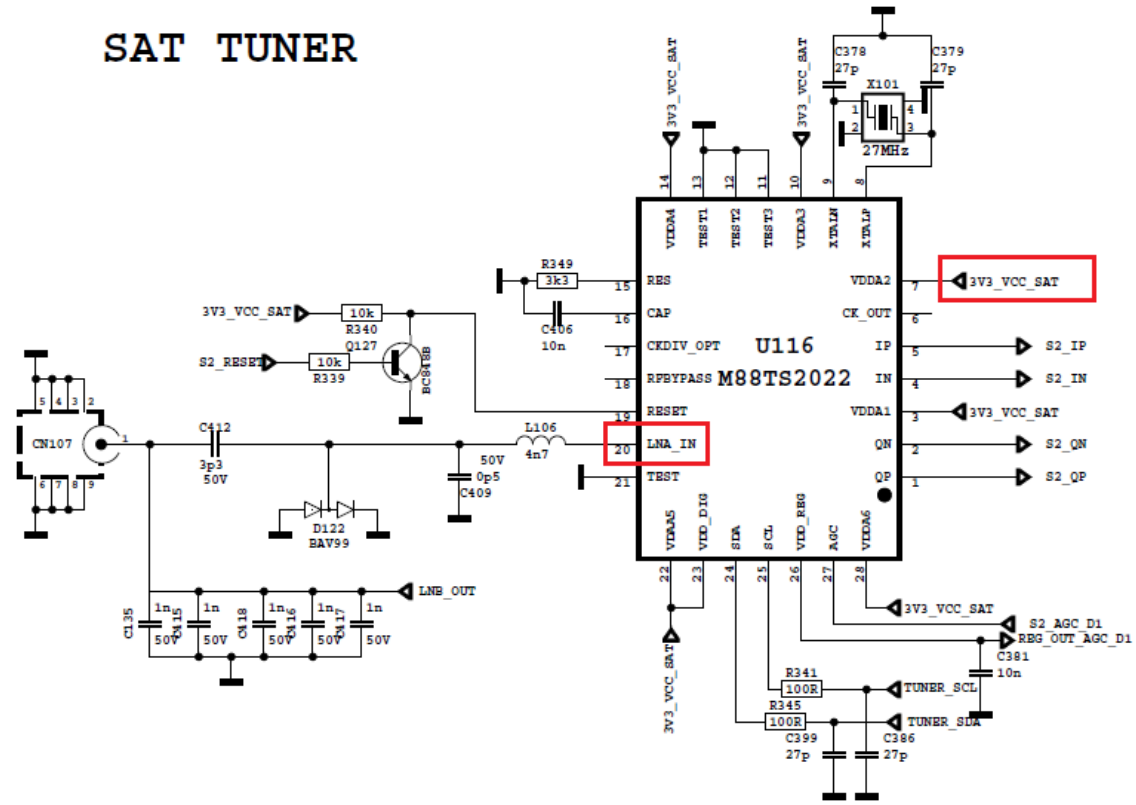
I. NO SIGNAL PROBLEM

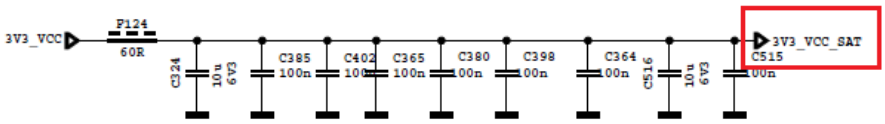
Problem: No signal or Low signal in DVB-S/S2 mode.

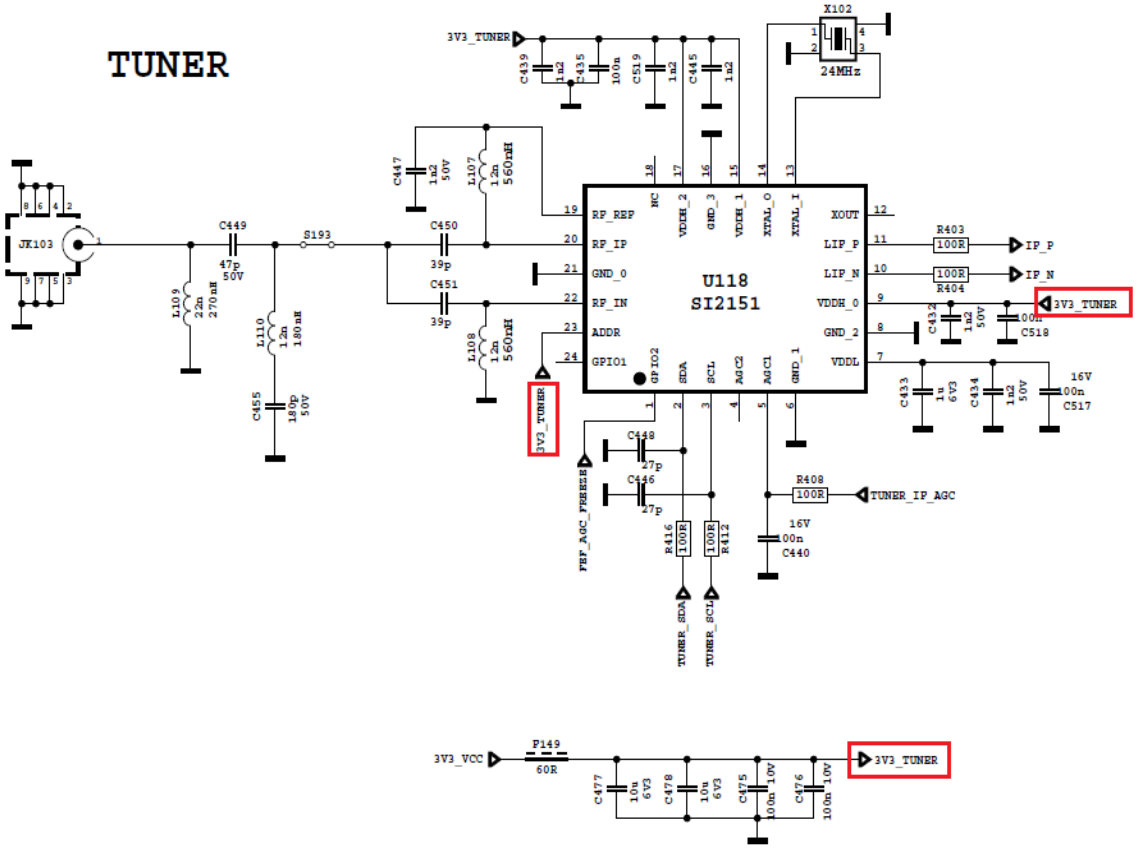
Check signal cables and LNB voltage, if there is no problem, check M88TS2022 (U116) supply voltages; 3V3_VCC_SAT.

If the above measurements are OK, then measure the voltage from the PIN20 of U116.

If the PIN1 voltage is equal to 0V, please check i2c waveforms and software. If the PIN1 voltage is lower than 1V(e.g: 0.8Vor 0.3V), change the U116 with a new part.


SAT TUNER
U116
M88TS2022
3V3_VCC_SAT
S2_RESET
S2_IP
S2_IN
S2_QN
S2_QP
LNB_OUT
S2_AGC_D1
RBG_OUT_AGC_D1
TUNER_SCL
TUNER_SDA
27MHz
CN107
D122
BAV99

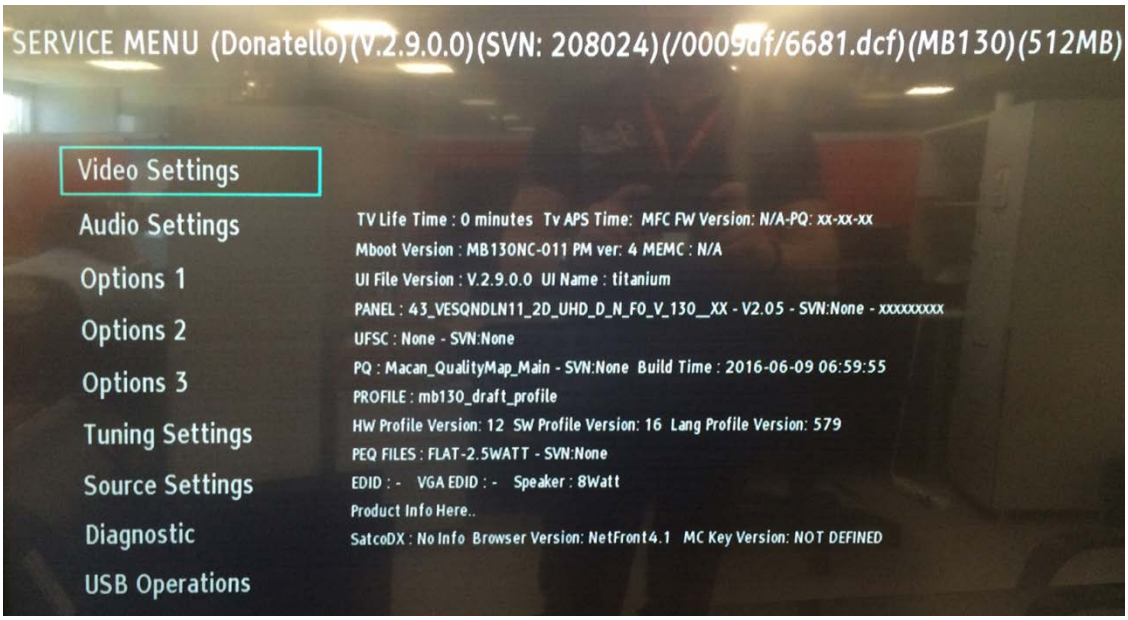

3V3_VCC
3V3_VCC_SAT


TUNER
U118
SI2151
3V3_TUNER
IP_P
IP_N
TUNER_IP_AGC
24MHz
JK103

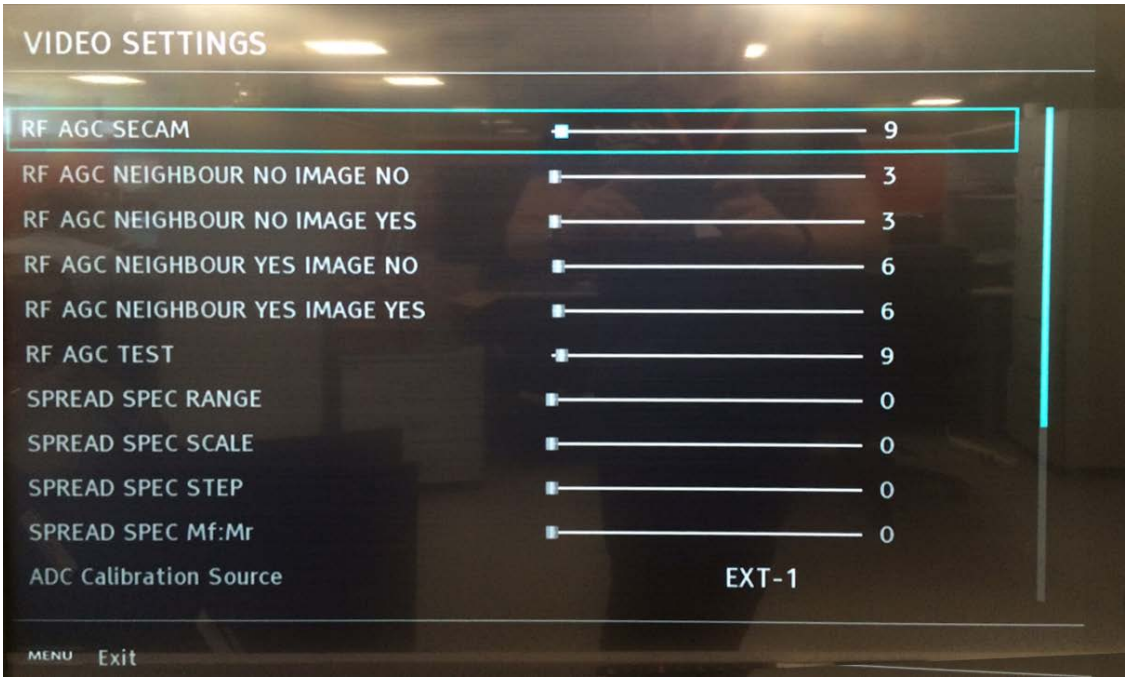
3V3_VCC
3V3_TUNER

14. SERVICE MENU SETTINGS

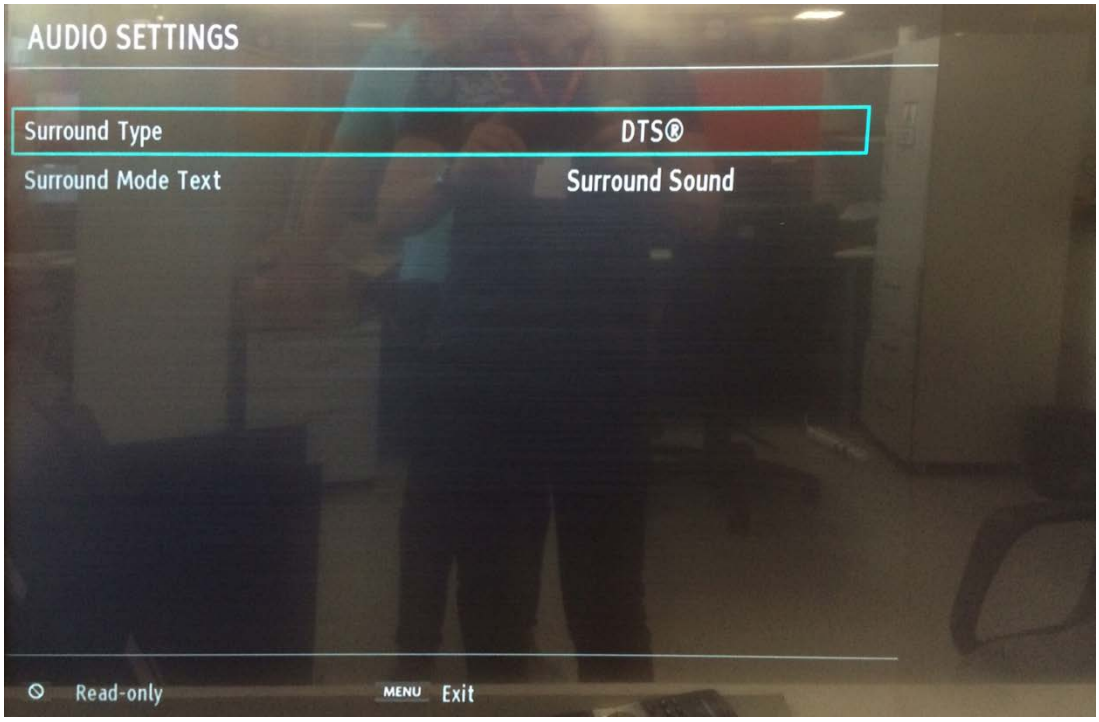
In order to reach service menu, first Press **“MENU”** buton, then write “**4725”** by using remote controller. You can see the service menu main screen below. You can check SW releases by using this menu. In addition, you can make changes on video, audio etc. by using video settings, audio settings titles.



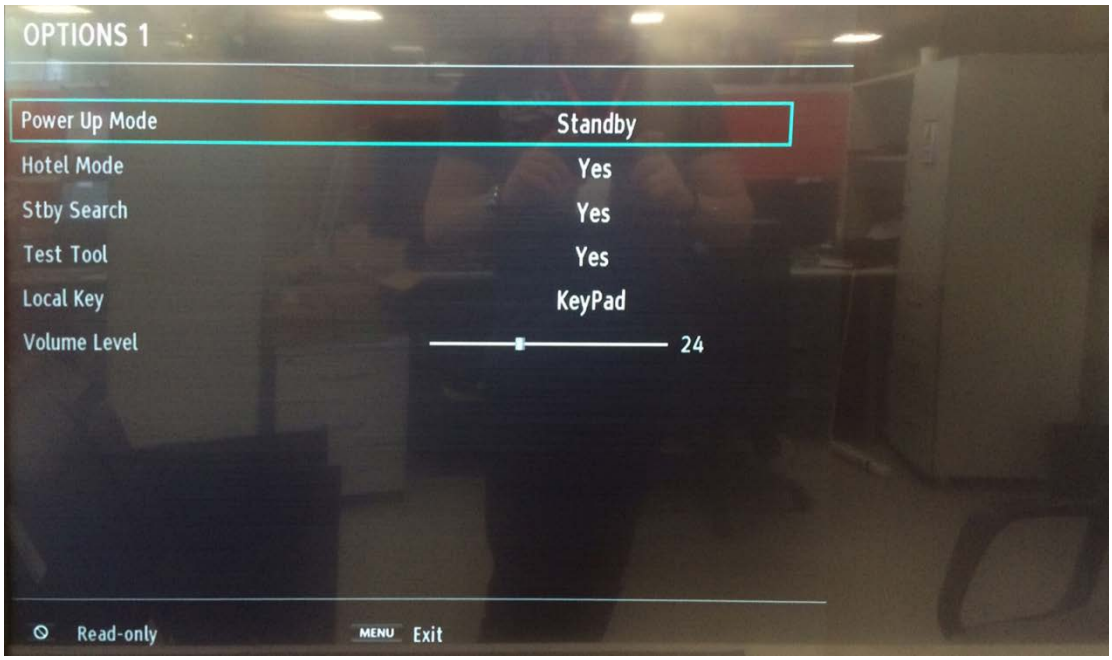
Service Menu



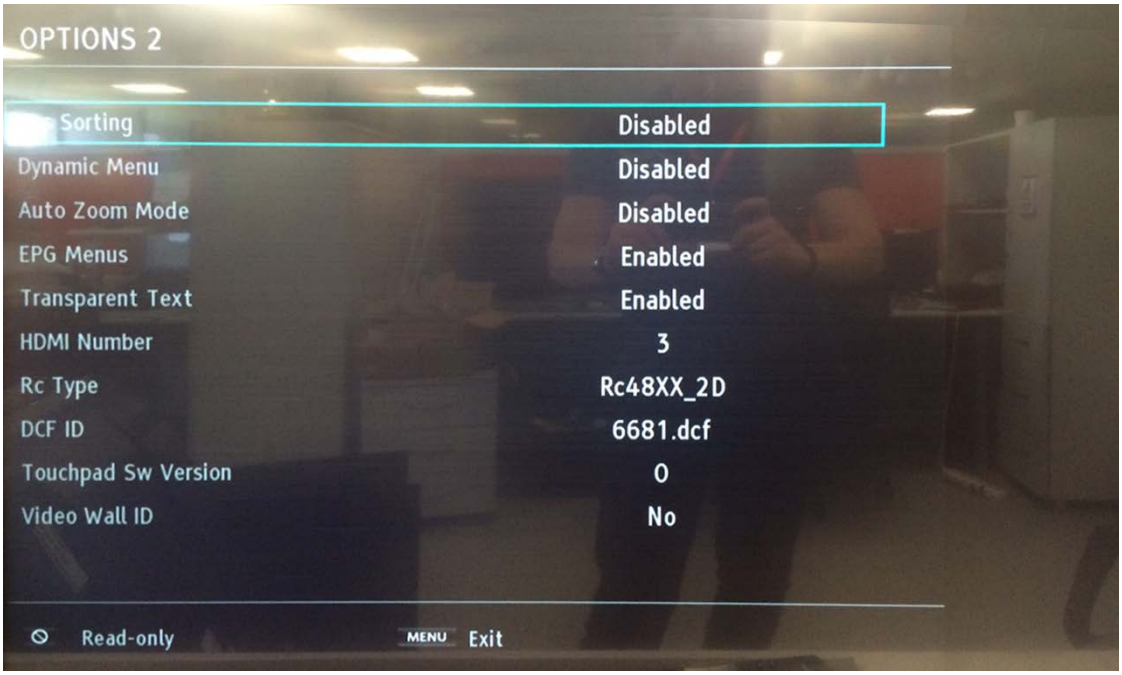
Video Settings



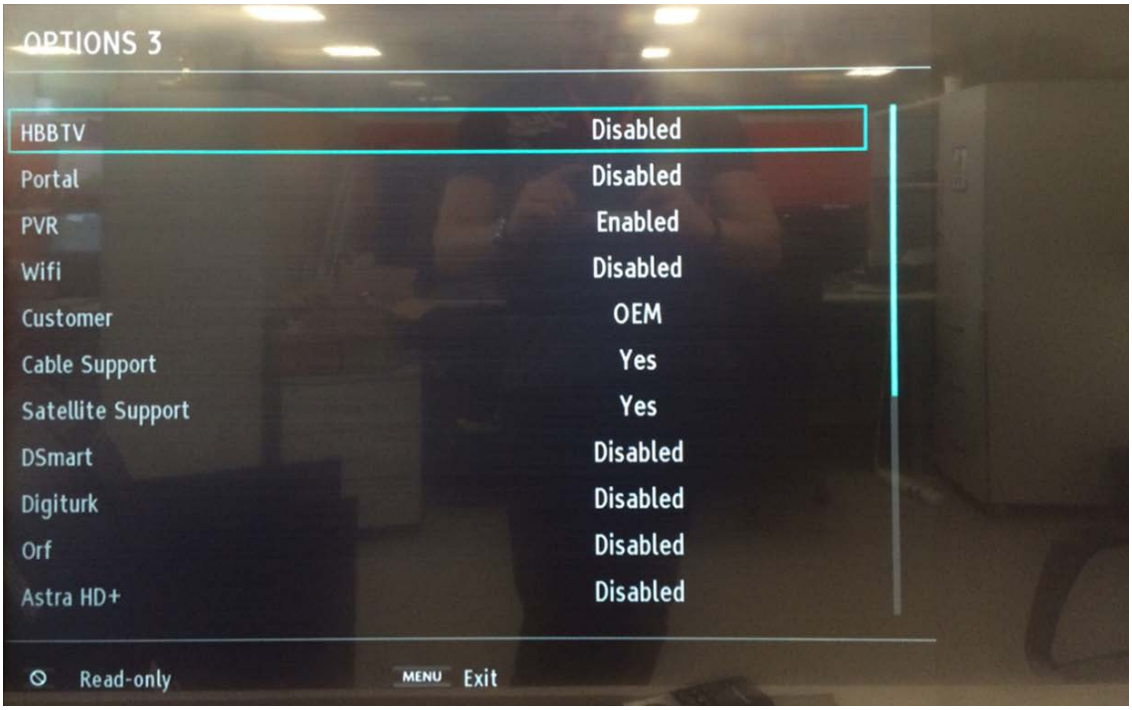
Audio Settings



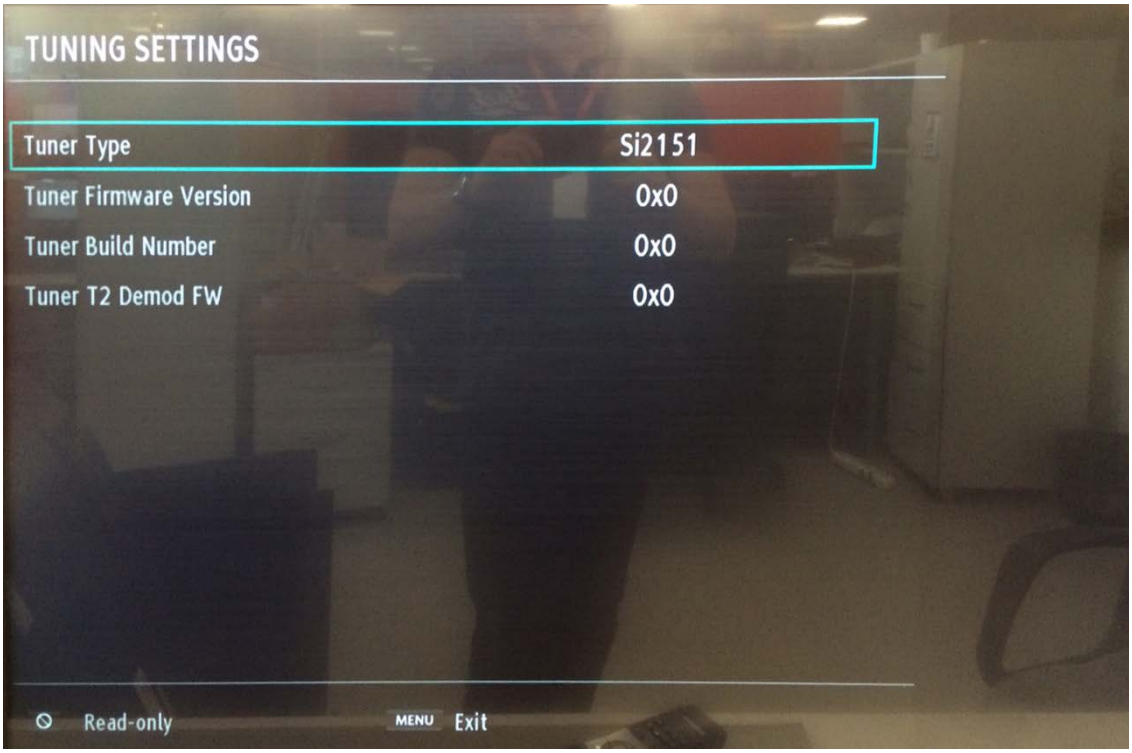
Options 1



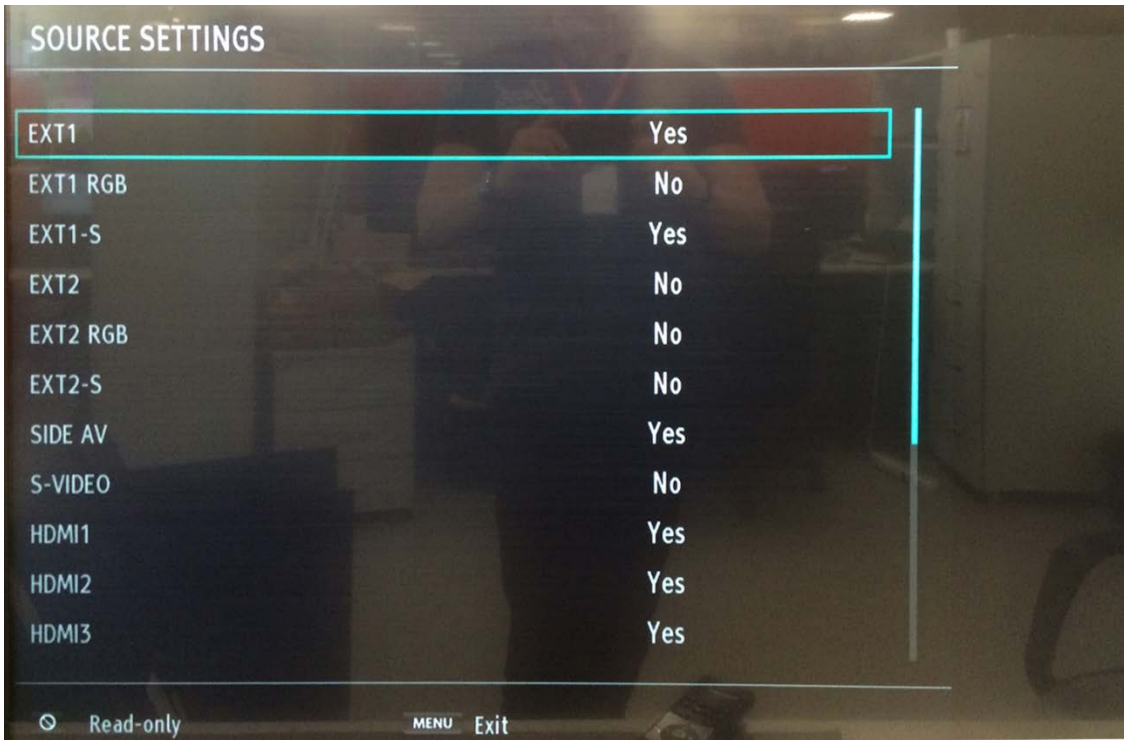
Options 2



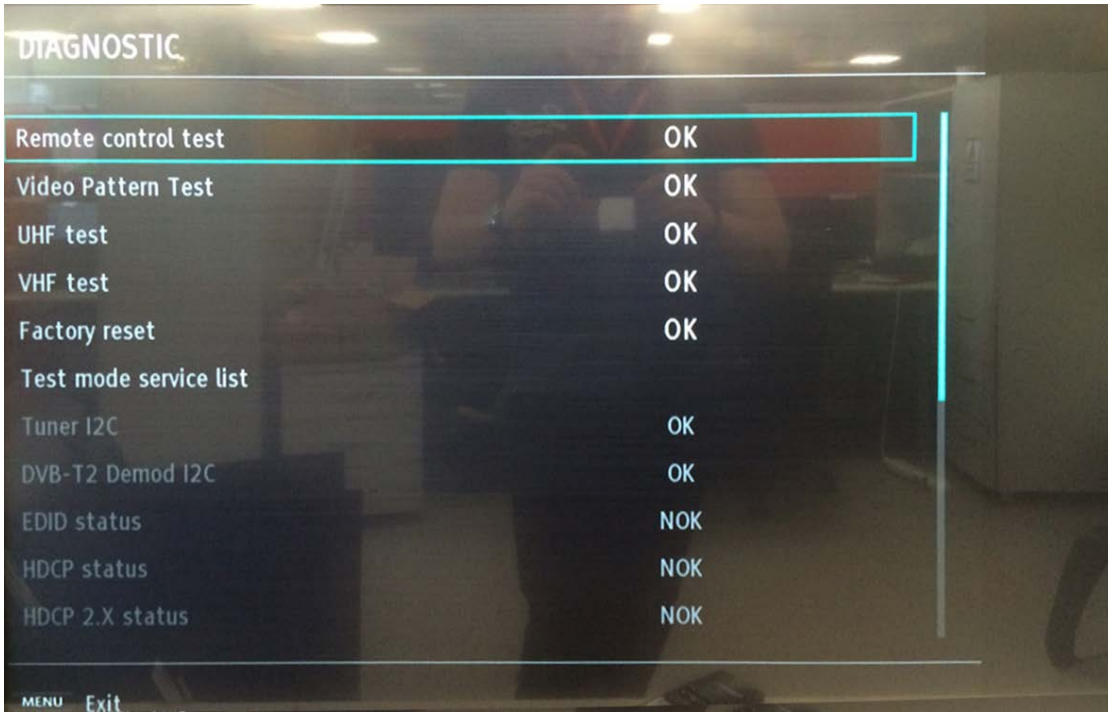
Options 3



Tuning Settings



Source Settings


DIAGNOSTIC
Remote control test
OK
Video Pattern Test
OK
UHF test
OK
VHF test
OK
Factory reset
OK
Test mode service list
Tuner I2C
OK
DVB-T2 Demod I2C
OK
EDID status
NOK
HDCP status
NOK
HDCP 2.X status
NOK
MENU Exit

Diagnostic