



SERVICE MANUAL

MODELS : RHT497H/RHT499H

DVB-T/HDD/DVD RECORDER

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CAUTION

BEFORE SERVICING THE UNIT, READ THE "SAFETY PRECAUTIONS"
IN THIS MANUAL.



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SECTION 1

SUMMARY

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NEW FUNCTIONS OF DVB-T/HDD/DVD RECORDER

• HDMI

HDMI IS THE SPECIFICATION FOR THE HIGH-DEFINITION MULTIMEDIA INTERFACE. HDMI IS PROVIDED FOR TRANSMITTING DIGITAL TELEVISION AUDIOVISUAL SIGNALS FROM HDD-DVD RECORDER TO TELEVISION SETS, OTHER VIDEO DISPLAYS. HDMI CAN CARRY HIGH QUALITY MULTI-CHANNEL AUDIO DATA AND CAN CARRY ALL STANDARD AND HIGH DEFINITION CONSUMER ELECTRONICS VIDEO FORMATS. CONTENT PROTECTION TECHNOLOGY IS AVAILABLE. HDMI CAN ALSO CARRY CONTROL AND STATUS INFORMATION IN BOTH DIRECTIONS.

<< OPERATING >>

AUDIO, VIDEO AND AUXILIARY DATA IS TRANSMITTED ACROSS THE THREE TMDS DATA CHANNELS. THE VIDEO PIXEL CLOCK IS TRANSMITTED ON THE TMDS CLOCK CHANNEL AND USED BY THE RECEIVER AS A FREQUENCY REFERENCE FOR DATA RECOVERY ON THE THREE TMDS DATA CHANNELS.

VIDEO DATA IS CARRIED AS A SERIES OF 24-BIT PIXELS ON THE THREE TMDS DATA CHANNELS.

TMDS ENCODING CONVERTS THE 8BIT PER CHANNEL INTO THE 10BIT DC-BALANCED.

VIDEO PIXEL RATES CAN RANGE FROM 25MHz TO 165MHz. THE VIDEO PIXELS CAN BE ENCODED IN EITHER RGB, YCbCr 4:4:4 OR YCbCr 4:2:2 FORMATS. IN ALL THREE CASES, UP TO 24 BITS PER PIXEL CAN BE TRANSFERRED.

FAST DUBBING

DUBBING MEANS A COPYING FUNCTION BETWEEN HDD TO DVD DISCS.

COPYING BETWEEN HDD TO DVD IS A COMPLETELY DIGITAL PROCESS AND THEREFORE INVOLVES NO LOSS OF QUALITY IN THE AUDIO OR VIDEO. SO THIS MEANS THAT COPYING CAN BE CARRIED OUT AT THE MAXIMUM SPEED POSSIBLE.

<< DUBBING SPEED RATE >>

NORMAL DUBBING : SPEED RATE MAX X1

FAST DUBBING : SPEED RATE MAX X4

WHEN FAST DUBBING FROM HDD TO DVD, THE SPEED OF COPYING DEPENDS ON THE RECODING MODE AND THE KIND OF USING THE DVD DISC, AND THIS MODE IS NOT AVAILABLE FOR EDITED VIDEO TITLE IN HDD.

WHEN FAST DUBBING FROM DVD TO HDD, ONLY AVAILABLE WHEN COPYING VR MODE DISC(DVD-RW) TO HDD, AND ONLY NORMAL DUBBING AVAILABLE WHEN COPYING VIDEO MODE DISC(DVD+RW/RW, DVD-R) TO HDD.

PRODUCT SAFETY SERVICING GUIDELINES FOR DVB-T/HDD/DVD RECORDER PRODUCTS

IMPORTANT SAFETY NOTICE

This manual was prepared for use only by properly trained audio-video service technicians.

When servicing this product, under no circumstances should the original design be modified or altered without permission from LG Corporation. All components should be replaced only with types identical to those in the original circuit and their physical location, wiring and lead dress must conform to original layout upon completion of repairs.

Special components are also used to prevent x-radiation, shock and fire hazard. These components are indicated by the letter "x" included in their component designators and are required to maintain safe performance. No deviations are allowed without prior approval by LG Corporation.

Circuit diagrams may occasionally differ from the actual circuit used. This way, implementation of the latest safety and performance improvement changes into the set is not delayed until the new service literature is printed.

CAUTION : Do not attempt to modify this product in any way. Never perform customized installations without manufacturer's approval. Unauthorized modifications will not only void the warranty, but may lead to property damage or user injury.

Service work should be performed only after you are thoroughly familiar with these safety checks and servicing guidelines.

GRAPHIC SYMBOLS



The exclamation point within an equilateral triangle is intended to alert the service personnel to important safety information in the service literature.



The lightning flash with arrowhead symbol within an equilateral triangle is intended to alert the service personnel to the presence of noninsulated "dangerous voltage" that may be of sufficient magnitude to constitute a risk of electric shock.



The pictorial representation of a fuse and its rating within an equilateral triangle is intended to convey to the service personnel the following fuse replacement caution notice:

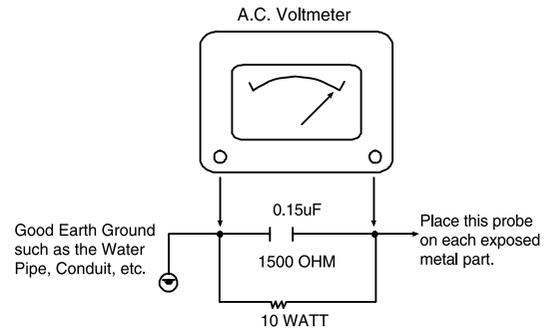
CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ALL FUSES WITH THE SAME TYPE AND RATING AS MARKED NEAR EACH FUSE.

SERVICE INFORMATION

While servicing, use an isolation transformer for protection from AC line shock. After the original service problem has been corrected, make a check of the following:

FIRE AND SHOCK HAZARD

1. Be sure that all components are positioned to avoid a possibility of adjacent component shorts. This is especially important on items transported to and from the repair shop.
2. Verify that all protective devices such as insulators, barriers, covers, shields, strain reliefs, power supply cords, and other hardware have been reinstalled per the original design. Be sure that the safety purpose of the polarized line plug has not been defeated.
3. Soldering must be inspected to discover possible cold solder joints, solder splashes, or sharp solder points. Be certain to remove all loose foreign particles.
4. Check for physical evidence of damage or deterioration to parts and components, for frayed leads or damaged insulation (including the AC cord), and replace if necessary.
5. No lead or component should touch a high current device or a resistor rated at 1 watt or more. Lead tension around protruding metal surfaces must be avoided.
6. After reassembly of the set, always perform an AC leakage test on all exposed metallic parts of the cabinet (the channel selector knobs, antenna terminals, handle and screws) to be sure that set is safe to operate without danger of electrical shock. **DO NOT USE A LINE ISOLATION TRANSFORMER DURING THIS TEST.** Use an AC voltmeter having 5000 ohms per volt or more sensitivity in the following manner: Connect a 1500 ohm, 10 watt resistor, paralleled by a .15 mfd 150V AC type capacitor between a known good earth ground water pipe, conduit, etc.) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination of 1500 ohm resistor and .15 mfd capacitor. Reverse the AC plug by using a non-polarized adaptor and repeat AC voltage measurements for each exposed metallic part. Voltage measured must not exceed 0.75 volts RMS. This corresponds to 0.5 milliamp AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.



TIPS ON PROPER INSTALLATION

1. Never install any receiver in a closed-in recess, cubbyhole, or closely fitting shelf space over, or close to, a heat duct, or in the path of heated air flow.
2. Avoid conditions of high humidity such as: outdoor patio installations where dew is a factor, near steam radiators where steam leakage is a factor, etc.
3. Avoid placement where draperies may obstruct venting. The customer should also avoid the use of decorative scarves or other coverings that might obstruct ventilation.
4. Wall- and shelf-mounted installations using a commercial mounting kit must follow the factory-approved mounting instructions. A product mounted to a shelf or platform must retain its original feet (or the equivalent thickness in spacers) to provide adequate air flow across the bottom. Bolts or screws used for fasteners must not touch any parts or wiring. Perform leakage tests on customized installations.
5. Caution customers against mounting a product on a sloping shelf or in a tilted position, unless the receiver is properly secured.
6. A product on a roll-about cart should be stable in its mounting to the cart. Caution the customer on the hazards of trying to roll a cart with small casters across thresholds or deep pile carpets.
7. Caution customers against using extension cords. Explain that a forest of extensions, sprouting from a single outlet, can lead to disastrous consequences to home and family.

SERVICING PRECAUTIONS

CAUTION: Before servicing the DVB-T/HDD/DVD RECORDER covered by this service data and its supplements and addends, read and follow the SAFETY PRECAUTIONS. NOTE: if unforeseen circumstances create conflict between the following servicing precautions and any of the safety precautions in this publications, always follow the safety precautions. Remember Safety First :

General Servicing Precautions

1. Always unplug the DVB-T/HDD/DVD RECORDER AC power cord from the AC power source before:
 - (1) Removing or reinstalling any component, circuit board, module, or any other assembly.
 - (2) Disconnecting or reconnecting any internal electrical plug or other electrical connection.
 - (3) Connecting a test substitute in parallel with an electrolytic capacitor.
Caution : A wrong part substitution or incorrect polarity installation of electrolytic capacitors may result in an explosion hazard.
2. Do not spray chemicals on or near this DVB-T/HDD/DVD RECORDER or any of its assemblies.
3. Unless specified otherwise in this service data, clean electrical contacts by applying an appropriate contact cleaning solution to the contacts with a pipe cleaner, cotton-tipped swab, or comparable soft applicator. Unless specified otherwise in this service data, lubrication of contacts is not required.
4. Do not defeat any plug/socket B+ voltage interlocks with which instruments covered by this service manual might be equipped.
5. Do not apply AC power to this DVB-T/HDD/DVD RECORDER and / or any of its electrical assemblies unless all solidstate device heat sinks are correctly installed.
6. Always connect the test instrument ground lead to an appropriate ground before connecting the test instrument positive lead. Always remove the test instrument ground lead last.

Insulation Checking Procedure

Disconnect the attachment plug from the AC outlet and turn the power on. Connect an insulation resistance meter (500V) to the blades of the attachment plug. The insulation resistance between each blade of the attachment plug and accessible conductive parts (Note 1) should be more than 1Mohm.

Note 1 : Accessible Conductive Parts include Metal panels, Input terminals, Earphone jacks, etc.

Electrostatically Sensitive (ES) Devices

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive (ES) Devices. Examples of typical ES devices are integrated circuits and some field effect transistors and semiconductor chip components.

The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ES devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded-tip soldering iron to solder or unsolder ES devices.
4. Use only an anti-static solder removal device. Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ES devices.
5. Do not use freon-propelled chemicals. These can generate an electrical charge sufficient to damage ES devices.
6. Do not remove a replacement ES device from its protective package until immediately before you are ready to install it. (Most replacement ES devices are packaged with leads electrically shorted together by conductive foam, aluminum foil, or comparable conductive material).
7. Immediately before removing the protective material from the leads of a replacement ES device, touch the protective material to the chassis or circuit assembly into which the device will be installed.

Caution: Be sure no power is applied to the chassis or circuit, and observe all other safety precautions.

8. Minimize bodily motions when handling unpackaged replacement ES devices. (Normally harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ES device.)

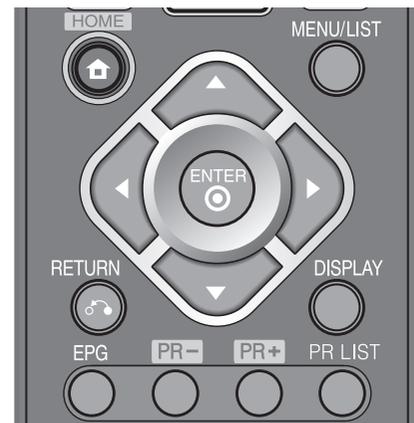
SERVICE INFORMATION FOR EEPROM IC SETTING

1. Press both "CLEAR" button on the Remocon and "▲ OPEN/CLOSE" button on the Front Panel about ±5 sec.



The picture on OSD will be as bellow :

[LGEDG / LGEHS]			
OP1 :	DA CA	00000000	
OP2 :	70 30	00000000	071102A
OP3 :	31 D1	00000000	
OP4 :	60 60	00000000	
OP5 :	0E 0E	00000000	
OP6 :	AA AA	00000000	
OP7 :	44 47	00000000	Write : OK
OP8 :	05 12	00000000	Exit : MP
OP9 :	0C 0C	00000000	Move : < >
OPA :	00 00	00000000	Edit : ▼ ▲
5			
Checksum of Option : 0x1105			
DVD read time : --- second			
CD read time : 10 sec -- > OK			

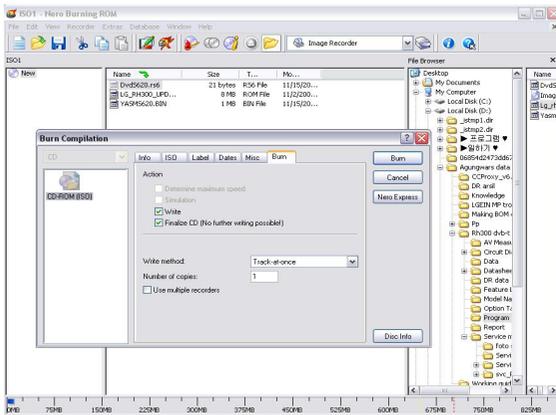


2. To MOVE from OP1 (Option 1) to another option, press ◀▶ button on the Remote Control.
3. To CHANGE the option code, press ▲▼ button on the Remote Control.
4. To APPLY the option Code, after change the option press OK/Enter button on Remote Control.
5. To INITIALIZE the system, press "CLEAR" button on the R/C together with "▲ OPEN/CLOSE" on the Front Panel about ±5 sec.
Note : This process will only clear the mapping channel and not delete data on HDD.
6. To exit from the option Code menu without Initialize the system, just turn off the power and then turn on again.

UPGRADE THE MAIN & LOADER PROGRAM

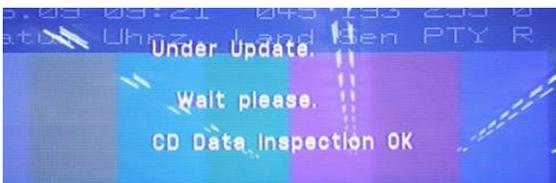
1. MAKING UPGRADE DISC MAIN SW AND LOADER SW

- 1) Do Physical format as ISO9660 or JOLIET file system
- 2) Don't care about the CD Volume label
- 3) Write Main SW file and Loader SW file on Root
 - ① Main SW file name is :
- LG_RH300_UPDATE_PAL.ROM
 - ② Loader SW file name is :
- DvdS620.rs6
- YASMS620

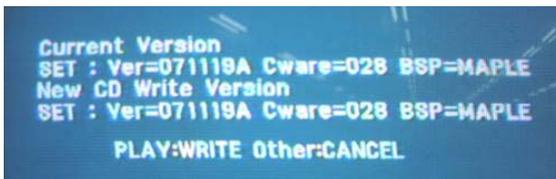


2. UPGRADE MAIN S/W

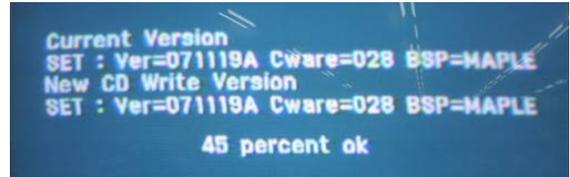
- 1) Insert Upgrade DISC into the Set
- 2) Press "DVD" button on the Remocon
- 3) After Disc Reading, CD Data Inspection Process. OSD like below :



- 4) If CD Data inspection OK, there will be message on OSD as below :



- 5) Press "PLAY" button to update S/W and another button to cancel.
- 6) Main S/W under updated. Do not turn off the power during updating process...!



- 7) If updating succeed, tray disc will be opened.



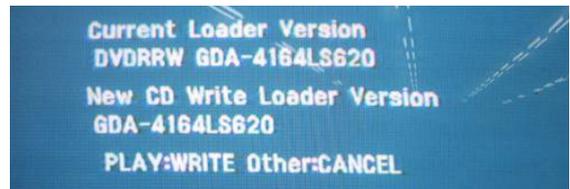
- 8) Turn on the power, and check the Main S/W Version.

3. UPGRADE LOADER S/W

- 1) Insert Upgrade DISC into the Set
- 2) Press "DVD" button on the Remocon
- 3) After Disc Reading, CD Data Inspection Process. OSD like below :

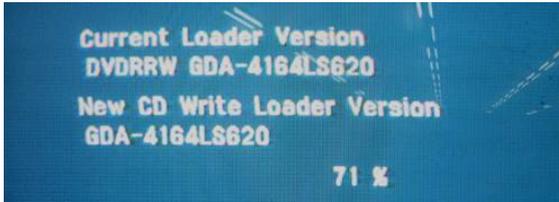


- 4) If CD Data inspection OK, there will be message on OSD as below :

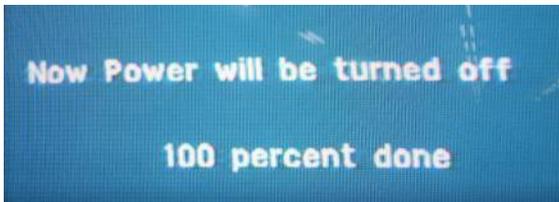


And Disc tray will be opened. Take off the disc

- 5) Press "PLAY" button to update S/W and another button to cancel.
- 6) Loader S/W under updated.
Do not turn off the power during updating process...!



If updating succeed, after completed there will be message :



Power will be automatically turn off.

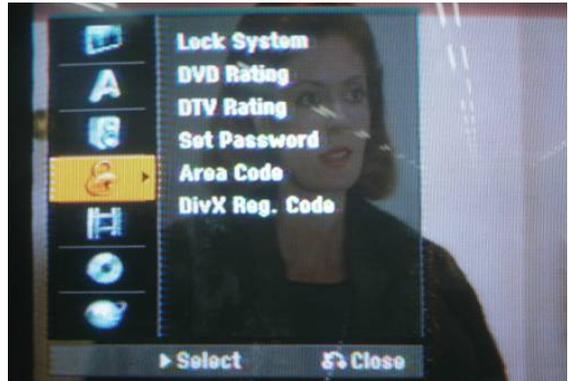
- 7) Turn on the power and check the Loader S/W Version.

4. S/W VERSION INFORMATION

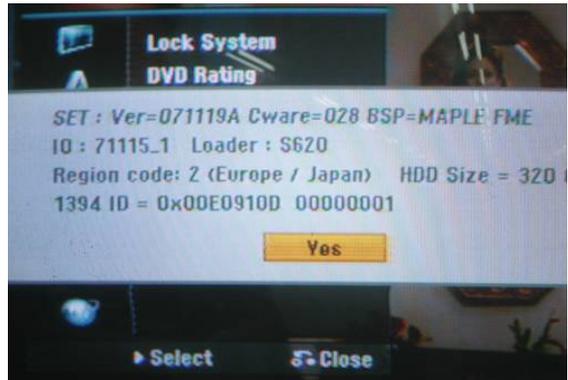
- 1) Press the "HOME" button on the Remocon
- 2) Select "EASY MENU" --> Select "SETUP"



- 3) Select menu "LOCK"



- 4) Press button number 7 - 8 - 8 - 9 on the Remocon
The picture on TV screen as below :



SPECIFICATIONS

• GENERAL

Power requirements	AC 200~240V, 50/60Hz
Power consumption	30W
Dimensions (approx.)	430 X 49 X 275mm (w x h x d) without foot
Net weight (approx.)	4kg
Operating temperature	5°C to 35°C
Operating humidity	5% to 65%
Television system	Analog: PAL I, B/G, I/I, SECAM D/K, K1 color system Digital: DVB-T Standard Compliant
Recording format	PAL

• RECORDING

Recording format	DVD Video Recording, DVD-VIDEO
Recordable media	HDD (RHT497H: 160GB, RHT498H: 250GB, RHT499H: 320GB), DVD-RW, DVD-R, DVD+RW, DVD+R, DVD+R(Double Layer), DVD-RAM DVD (4.7GB): Approx. 1 hour (XP mode), 2 hours (SP mode), 4 hours (LP mode), 6 hours (EP mode), 14 hours (MLP mode) DVD+R DL (8.5GB): Approx. 3 hours (XP mode), 3.8 hours (SP mode), 7.3 hours (LP mode), 9.1 hours (EP mode), 21 hours (MLP mode) HDD (160/250/320GB, MPEG2 Recording): Approx. 43/66/85 hours (XP mode), 84/129/165 hours (SP mode), 164/251/323 hours (LP mode), 233/356/456 hours (EP mode), 477/729/935 hours (MLP mode)
Recordable time	

Video recording format

Sampling frequency	27MHz
Compression format	MPEG2

Audio recording format

Sampling frequency	48kHz
Compression format	Dolby Digital

• PLAYBACK

Frequency response	DVD (PCM 48kHz): 8Hz to 22kHz, CD: 8Hz to 20kHz DVD (PCM 96kHz): 8Hz to 44kHz
Signal-to-noise ratio	More than 90dB (AUDIO OUT connector)
Harmonic distortion	Less than 0.02% (AUDIO OUT connector)

• INPUTS

ANTENNA IN	Antenna input, 75ohms
VIDEO IN	1.0Vp-p 75ohms, sync negative, RCA jack x 1 / SCART x 2
AUDIO IN	2.0Vrms more than 47kohms, RCA jack (L, R) x 1 / SCART x 2
DV IN	4 pin (IEEE 1394 standard)
USB IN	4 pin (USB 1.1 standard)

• OUTPUTS

VIDEO OUT	1Vp-p 75Ω, sync negative, SCART x 2
S-VIDEO OUT	(Y) 1.0V (p-p), 75Ω, sync negative, Mini DIN 4-pin x 1 (C) 0.3V (p-p) 75Ω
COMPONENT VIDEO OUT	(Y) 1.0V (p-p), 75Ω, sync negative, RCA jack x 1, (Pb)/(Pr) 0.7V (p-p), 75Ω, RCA jack x 2
HDMI video/audio output	19 pin (HDMI standard, Type A)
Audio output (digital audio)	0.5V (p-p), 75Ω, RCA jack x 1
Audio output (optical audio)	3V (p-p), Optical connector x 1
Audio output (analog audio)	2Vrms (1kHz, 0dB), 600Ω, RCA jack (L, R) x 2 / SCART x 2

SECTION 2

CABINET & MAIN CHASSIS

CONTENTS

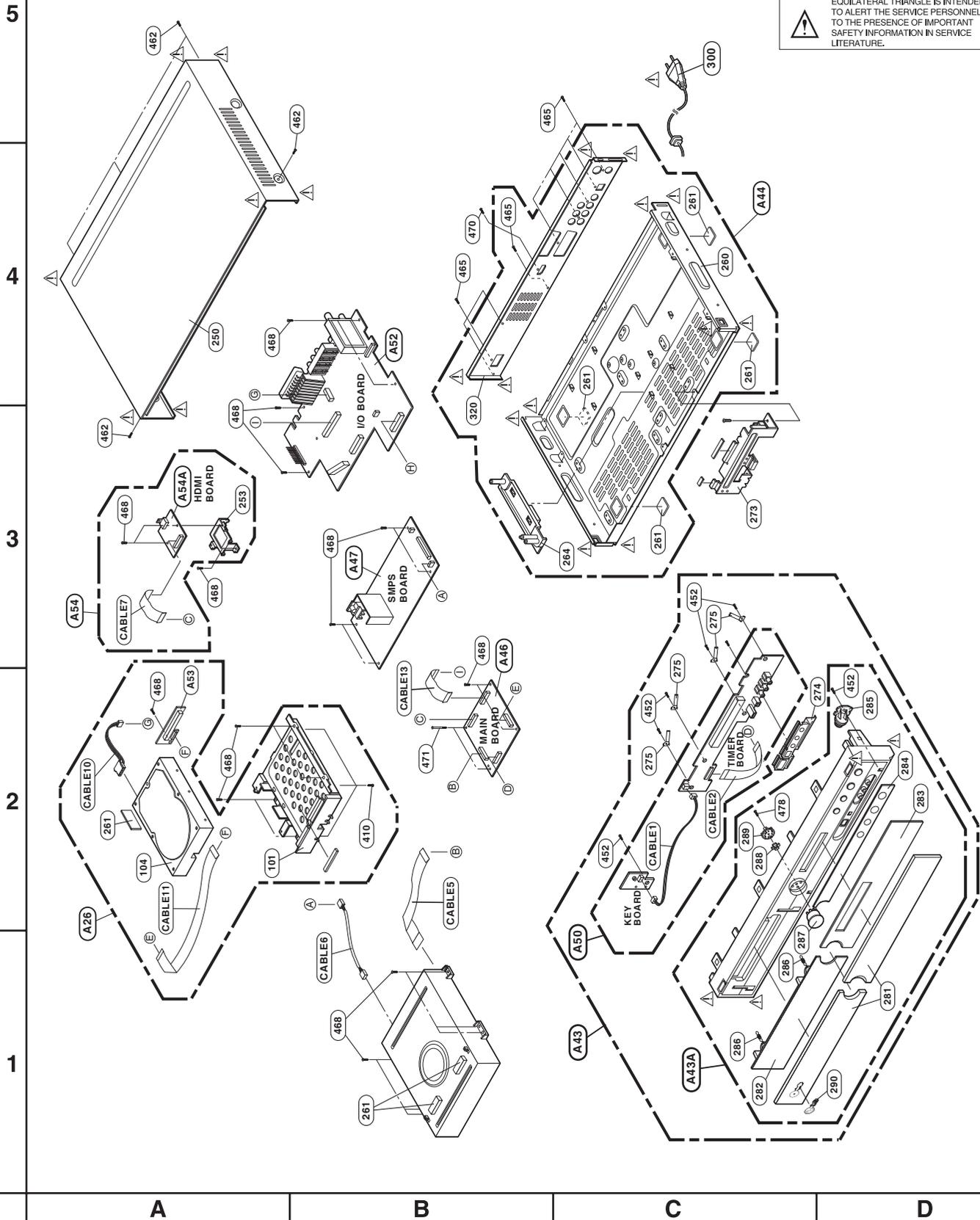
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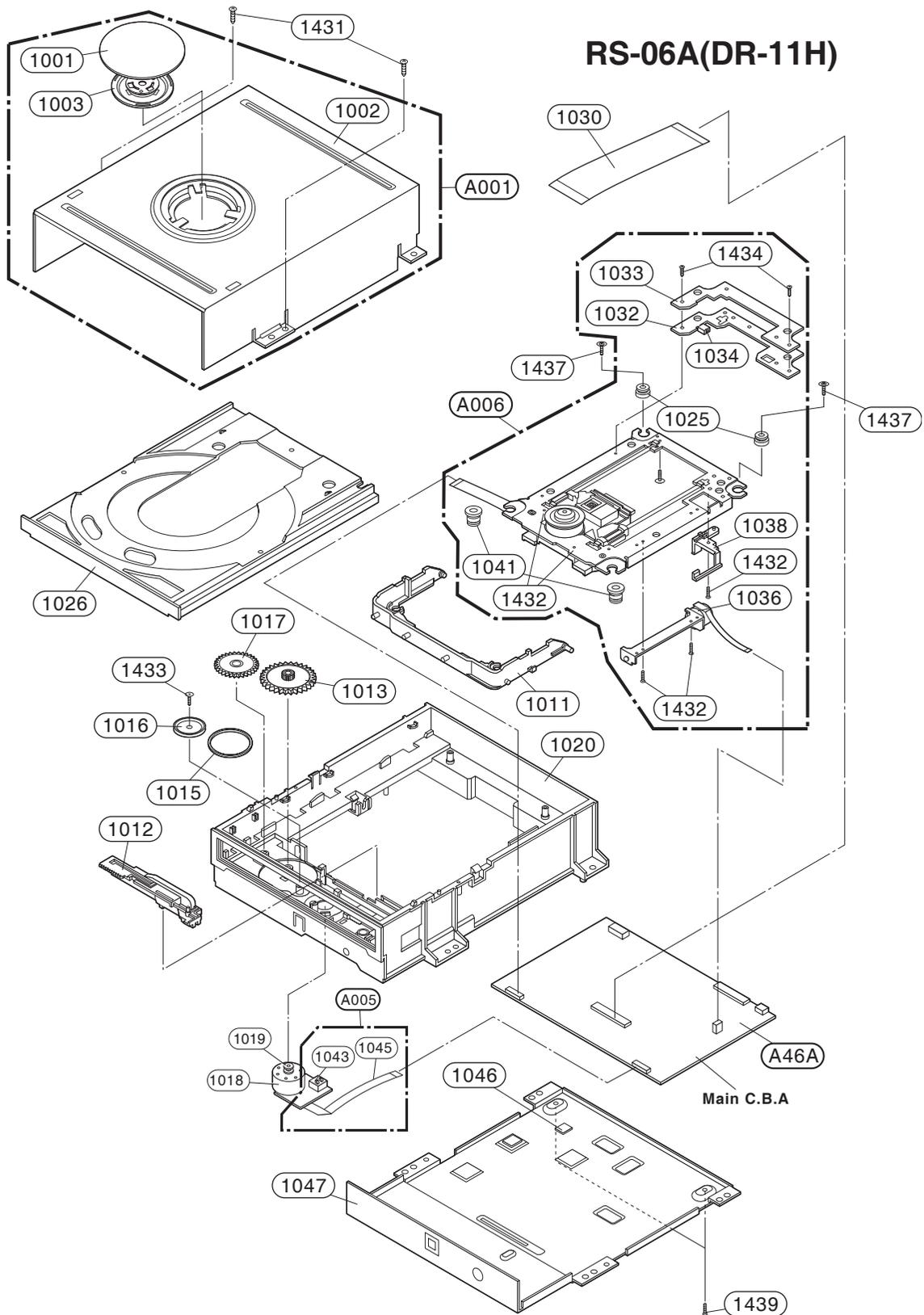
EXPLODED VIEWS

1. CABINET AND MAIN FRAME SECTION

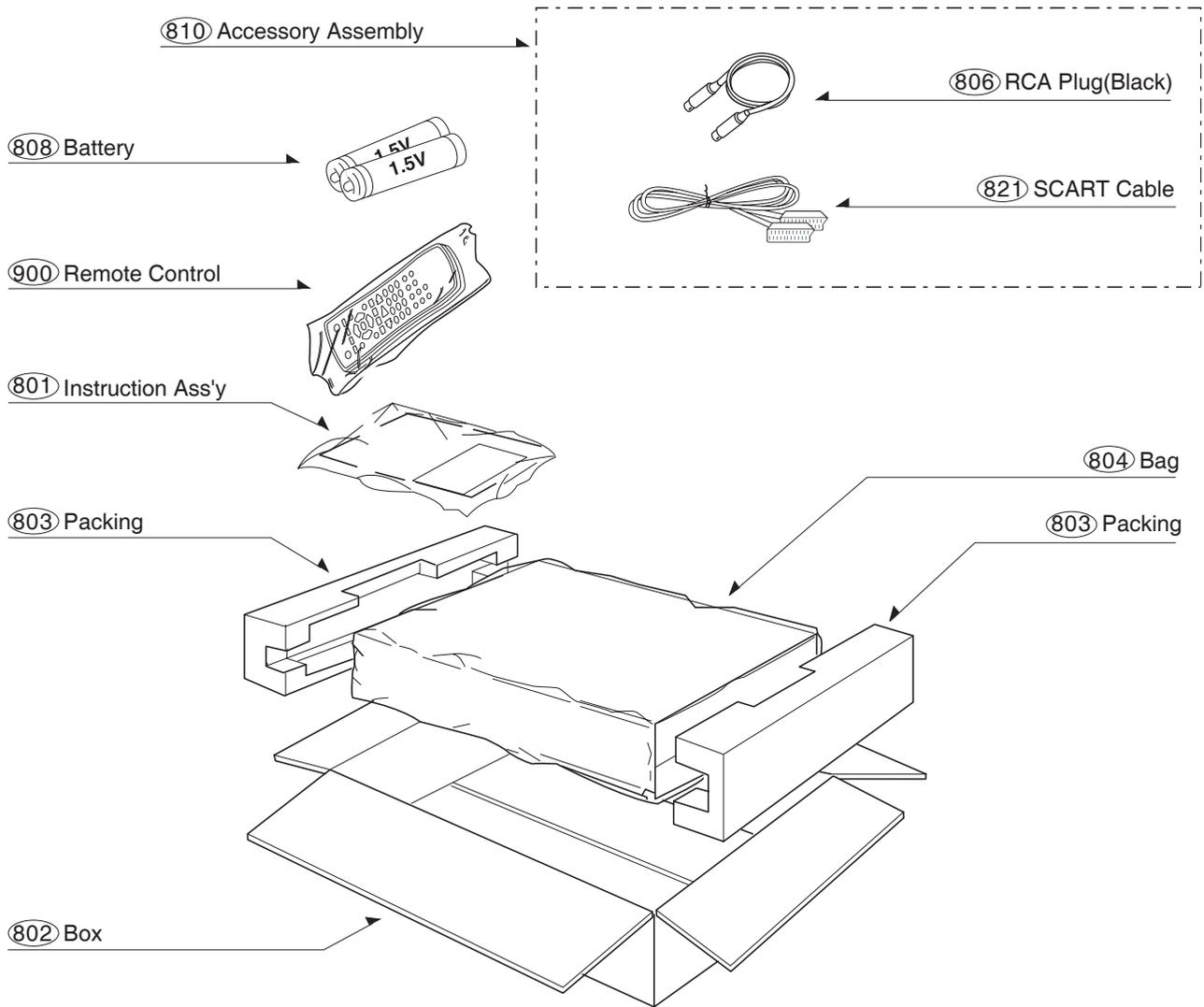
NOTES) THE EXCLAMATION POINT WITHIN AN EQUILATERAL TRIANGLE IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF IMPORTANT SAFETY INFORMATION IN SERVICE LITERATURE.



2. DECK MECHANISM SECTION (RS-06A)



3. PACKING ACCESSORY SECTION



SECTION 3

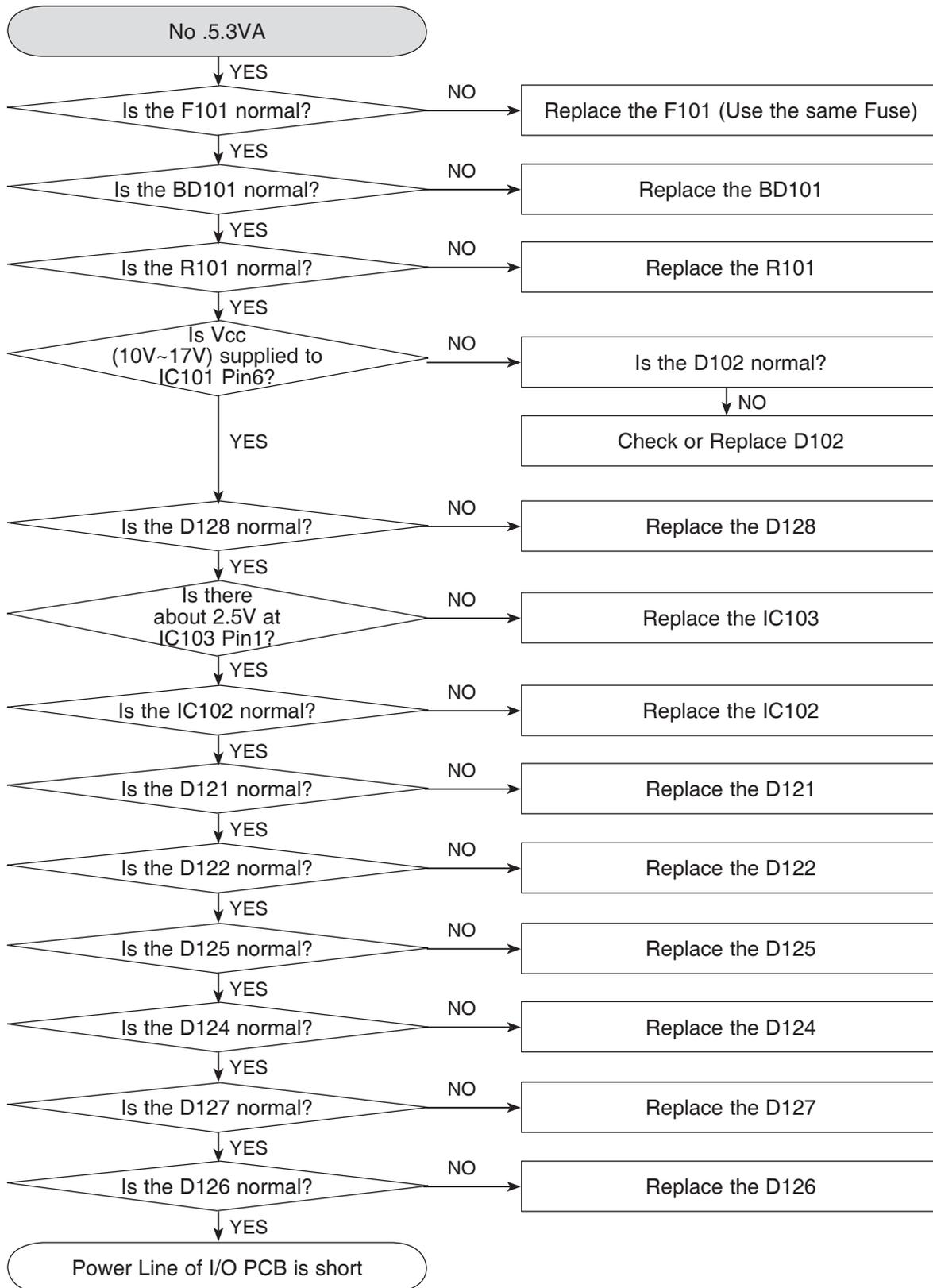
ELECTRICAL

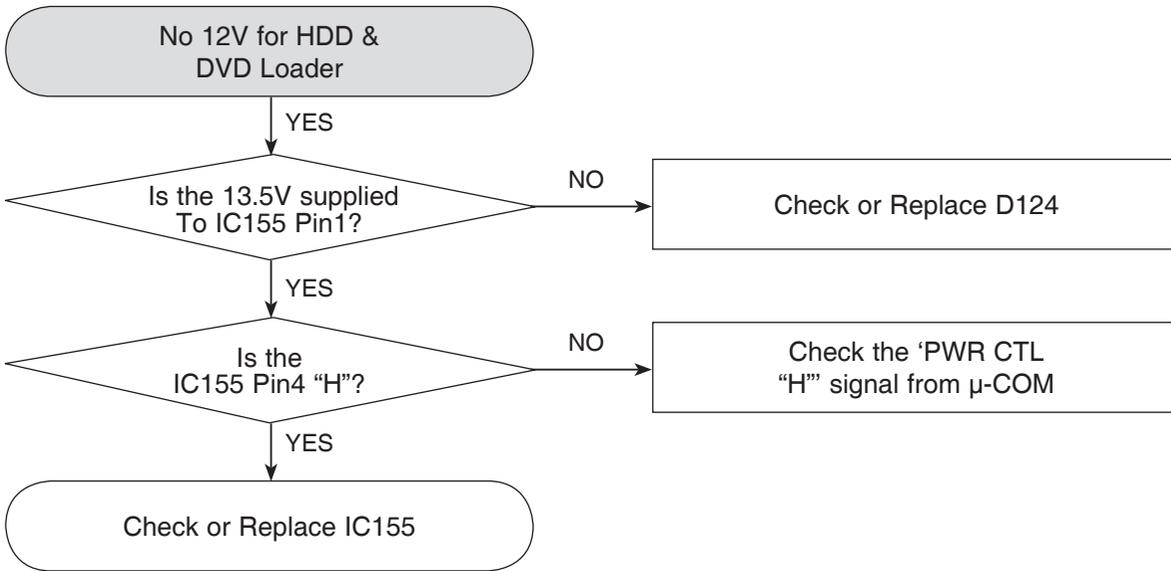
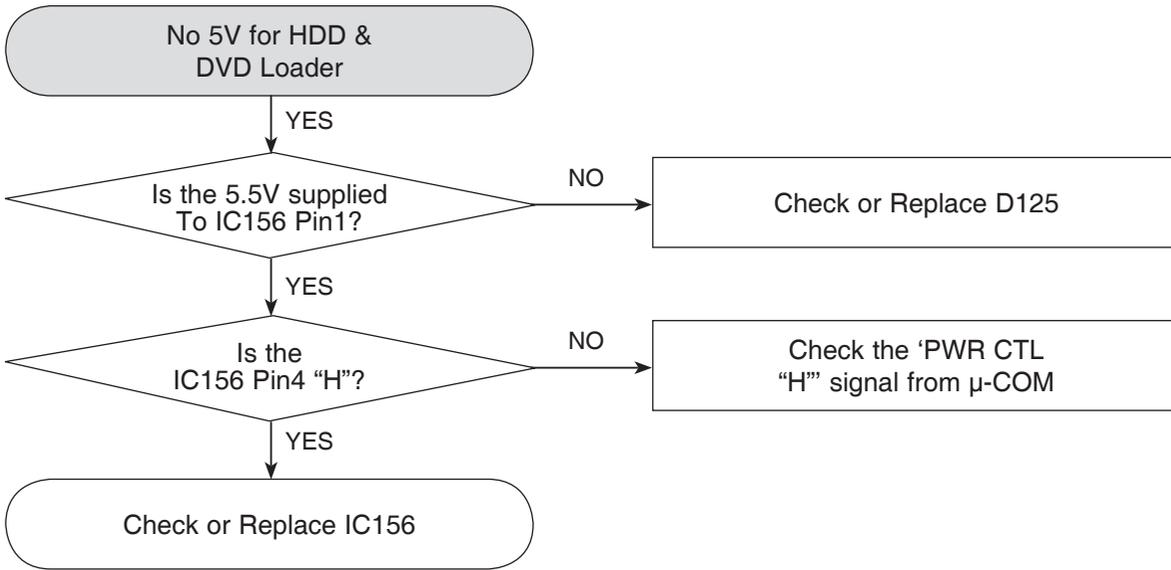
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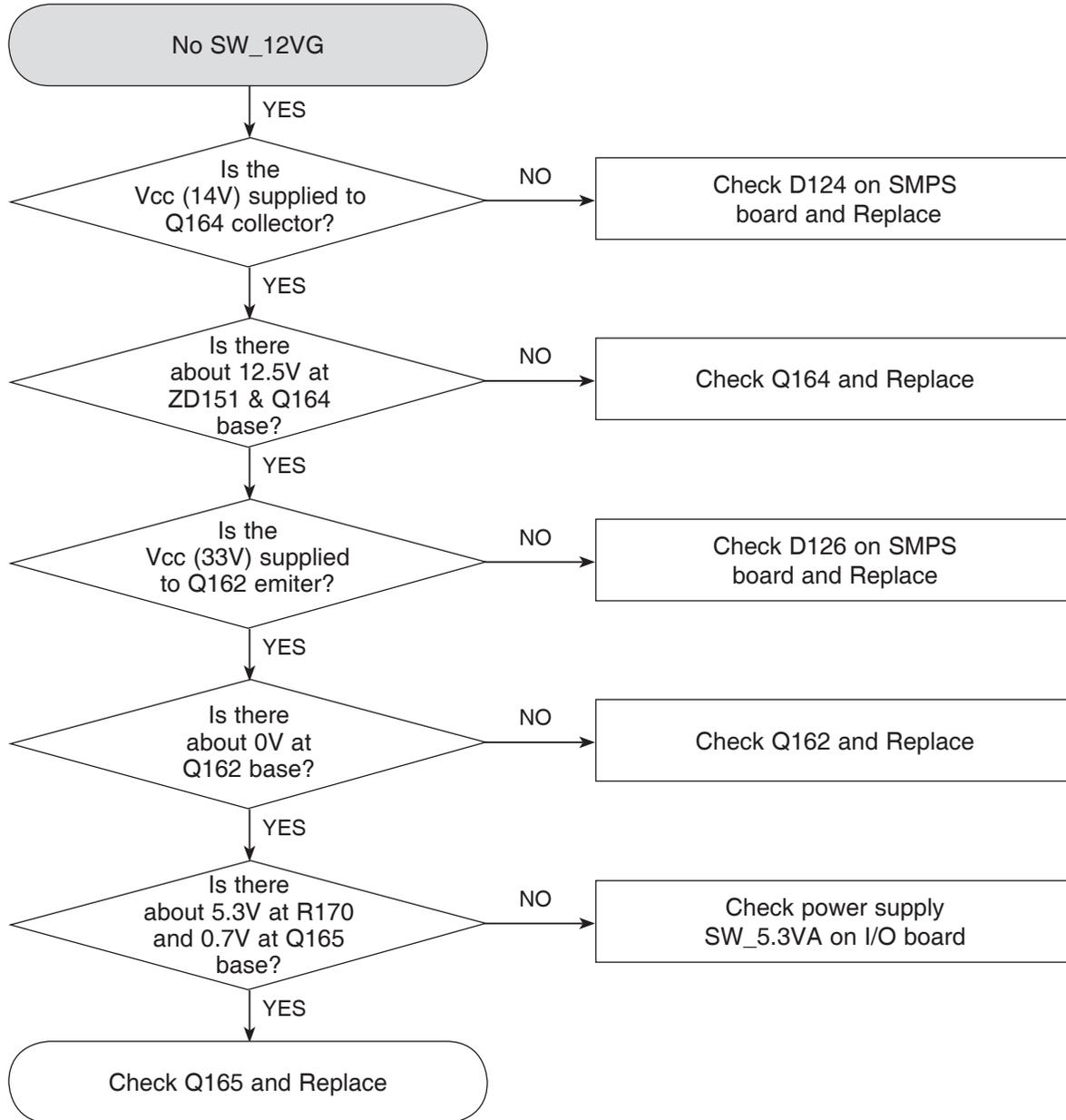
ELECTRICAL TROUBLESHOOTING GUIDE

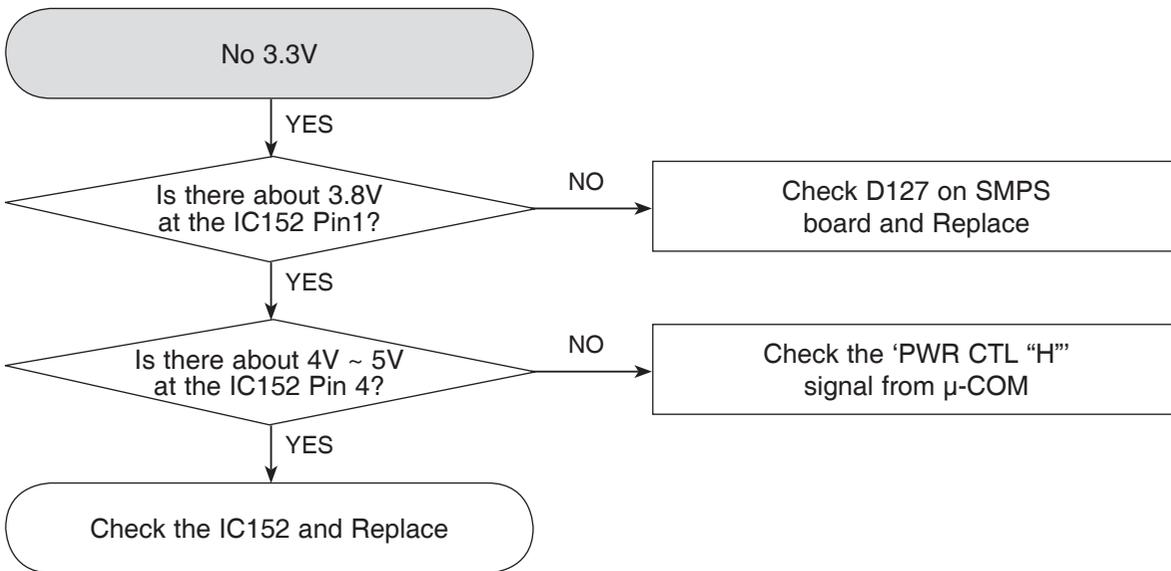
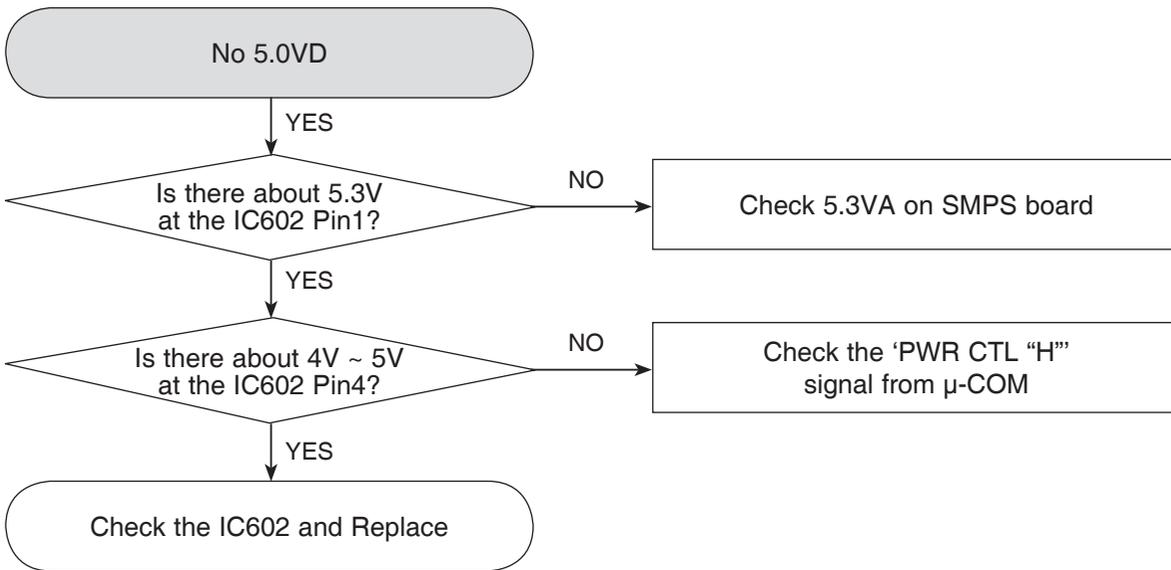
1. POWER SUPPLY ON SMPS BOARD

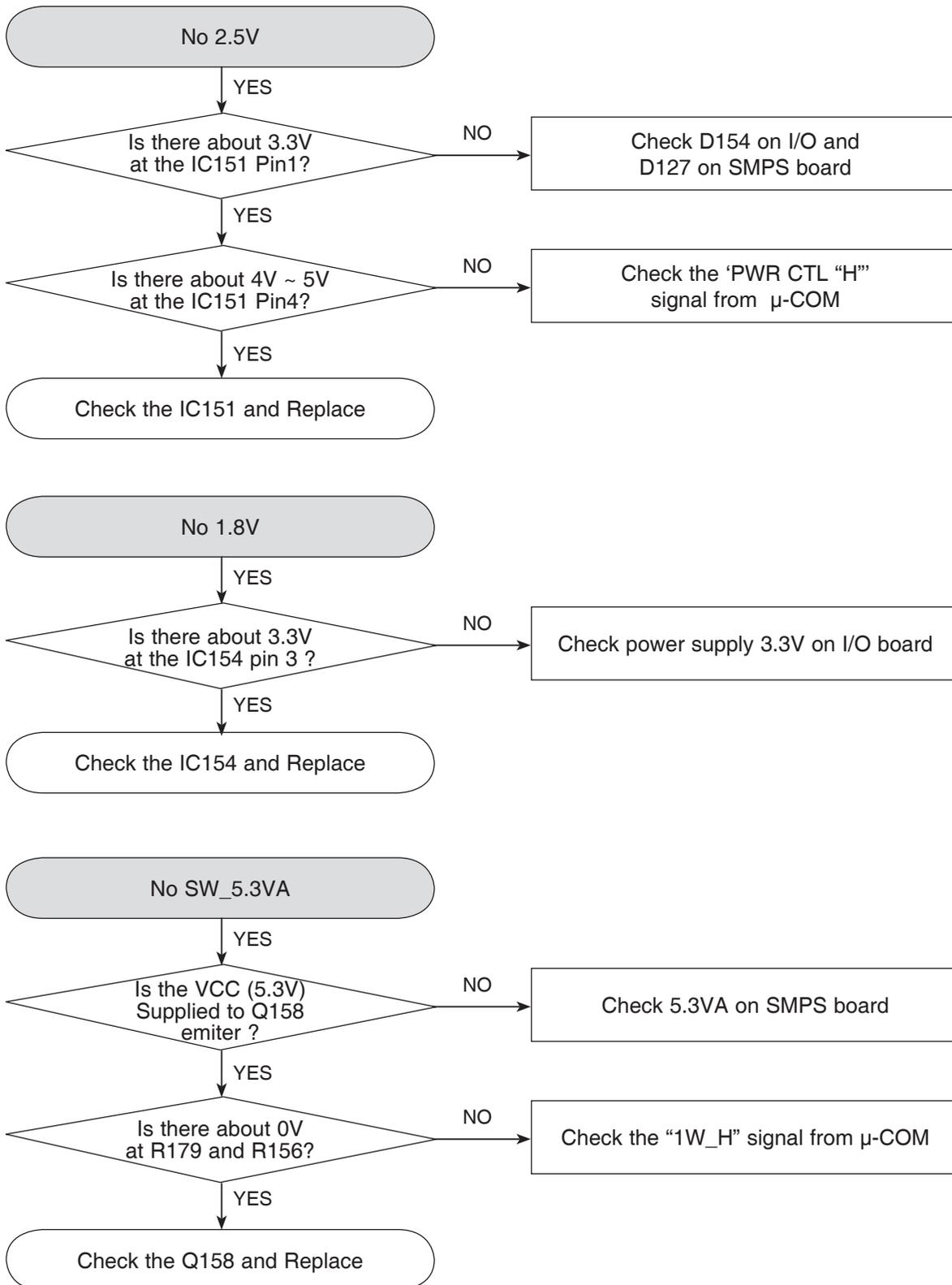


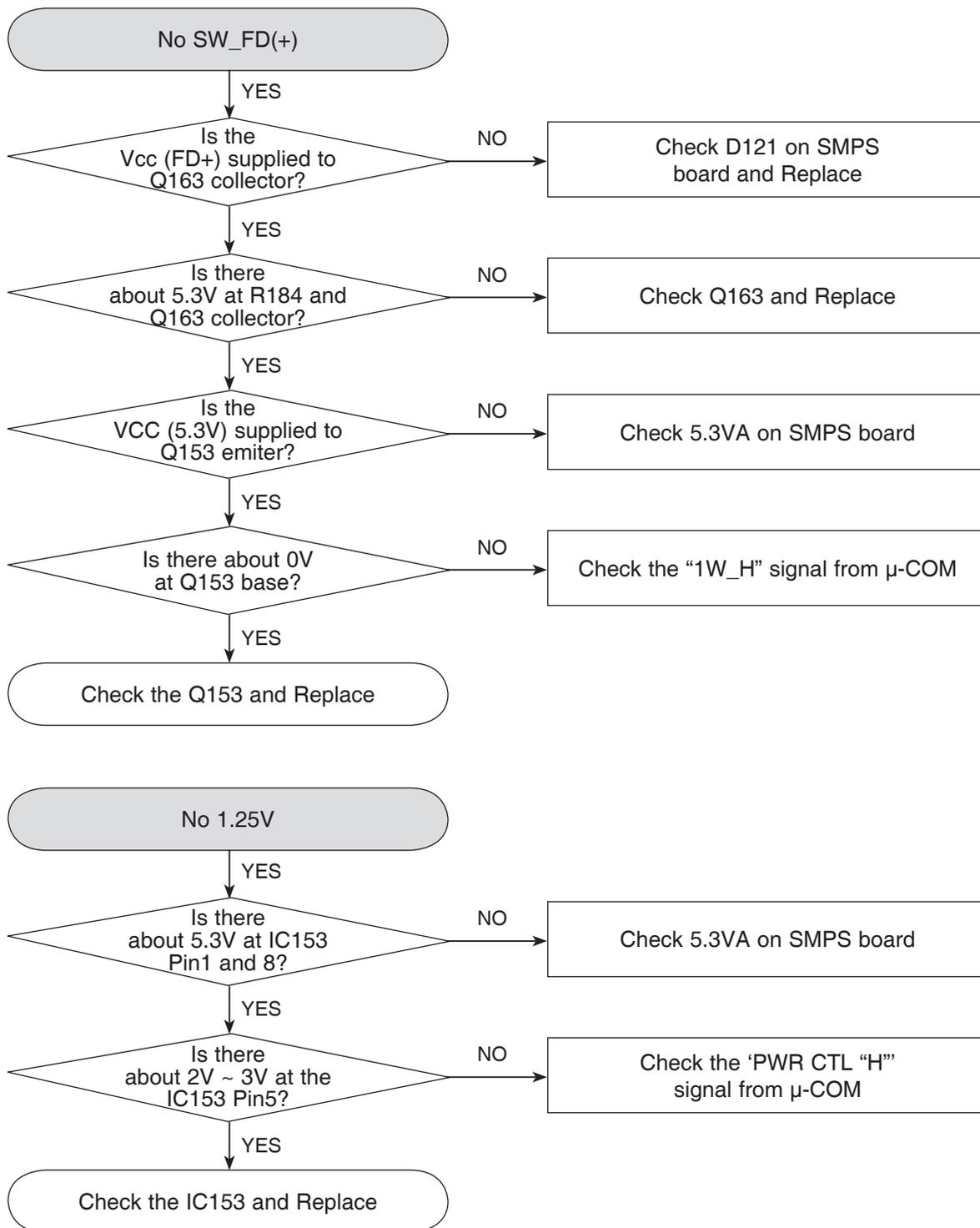


2. POWER SUPPLY ON I/O BOARD

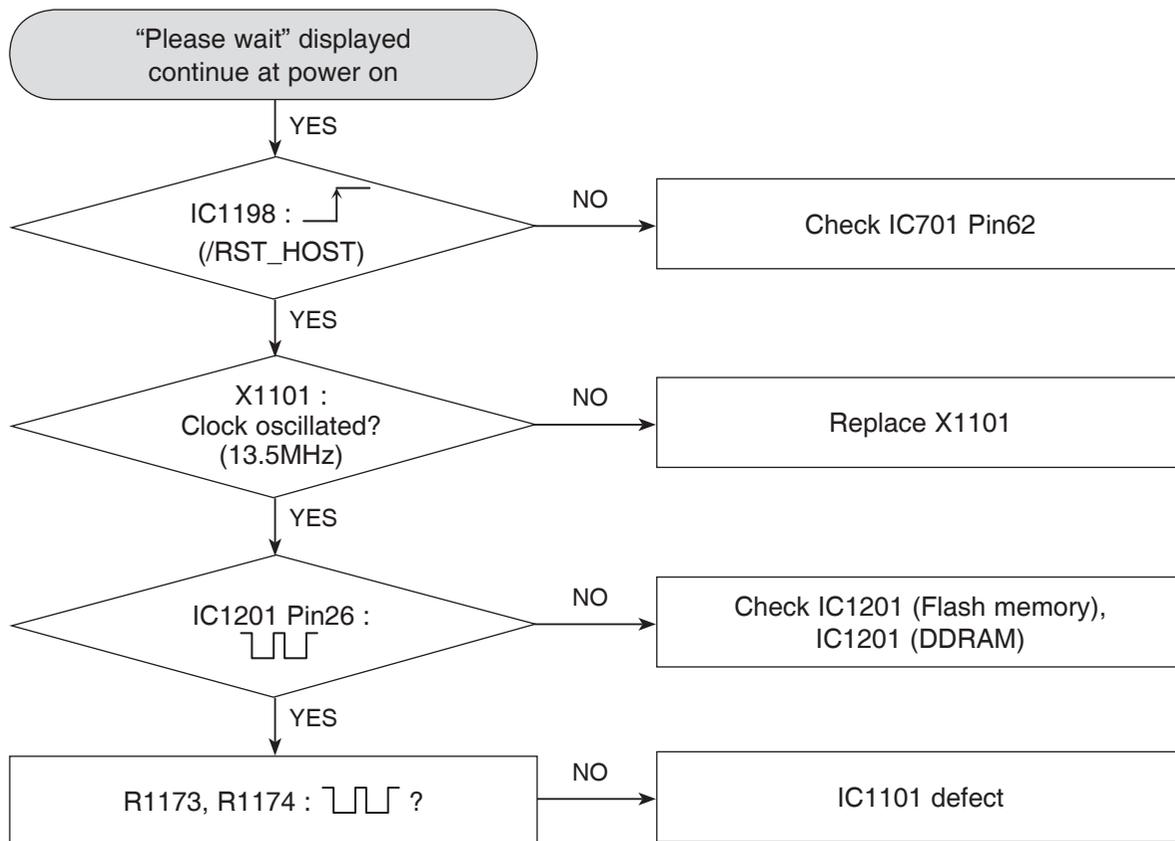




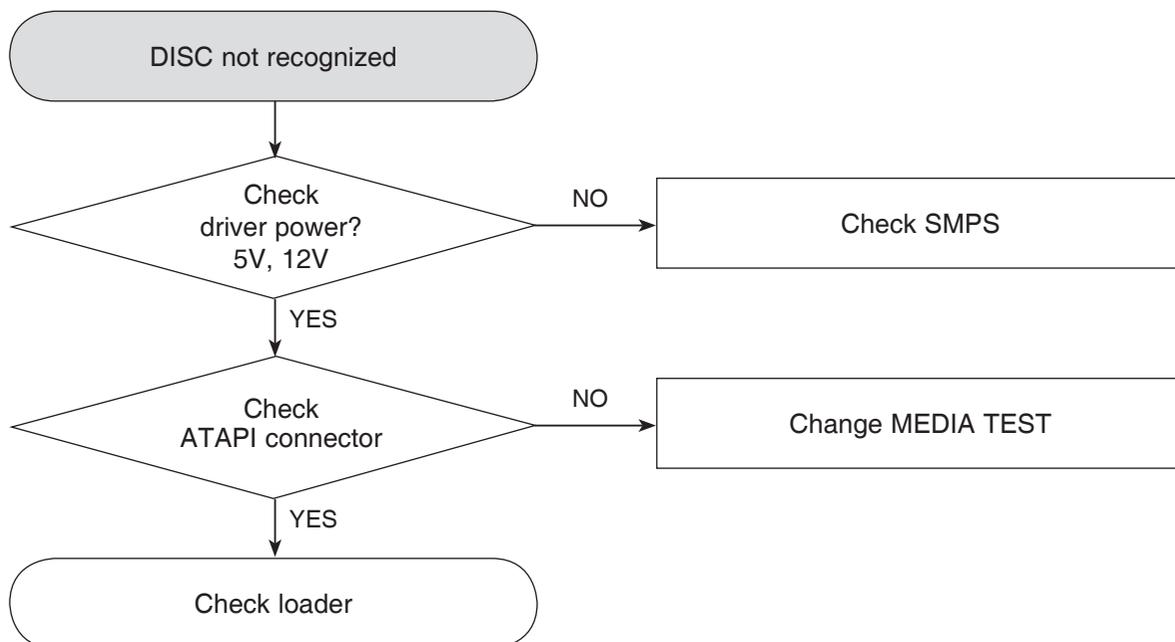




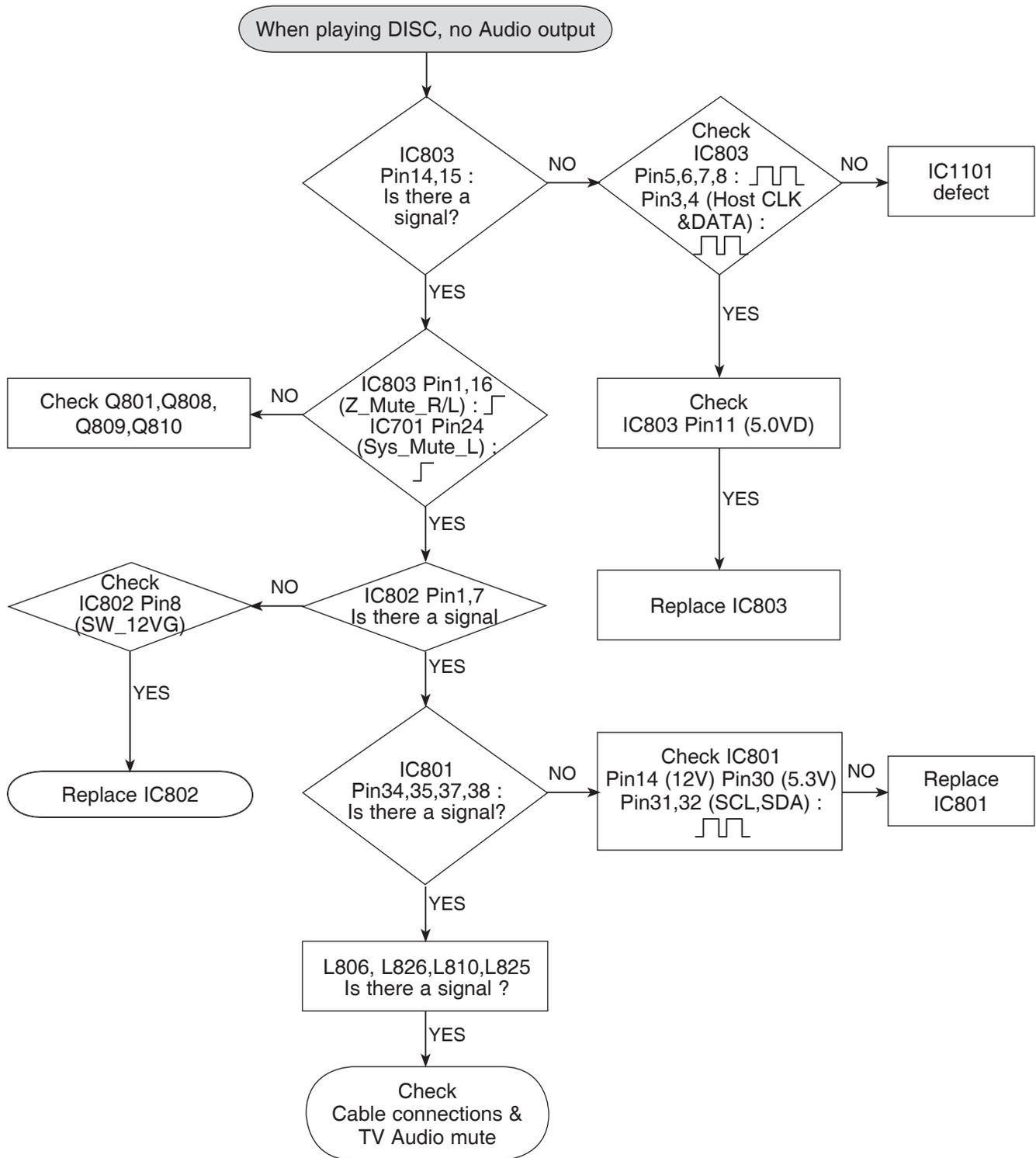
3. SYSTEM CIRCUIT PART



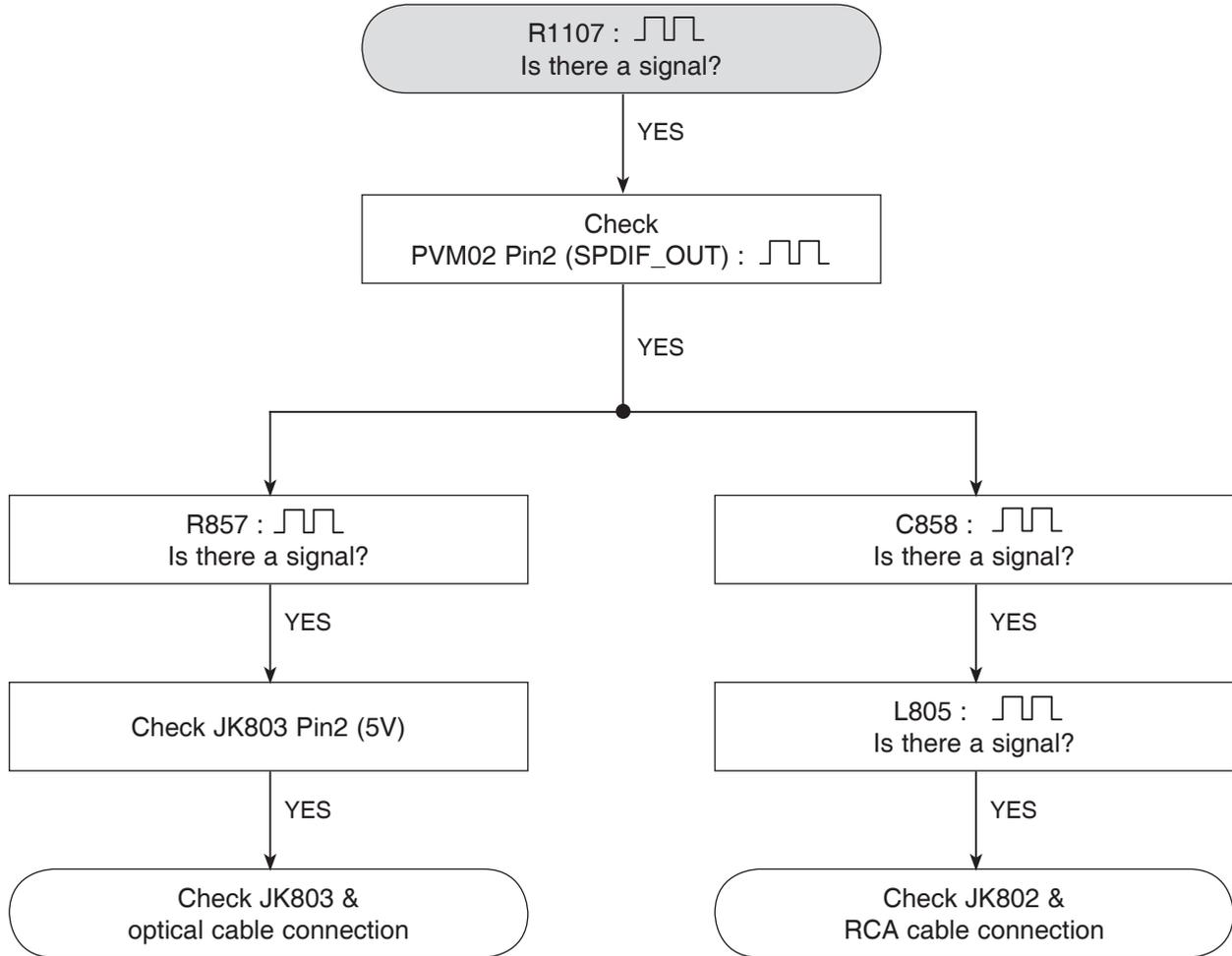
4. DISC NOT RECOGNIZED



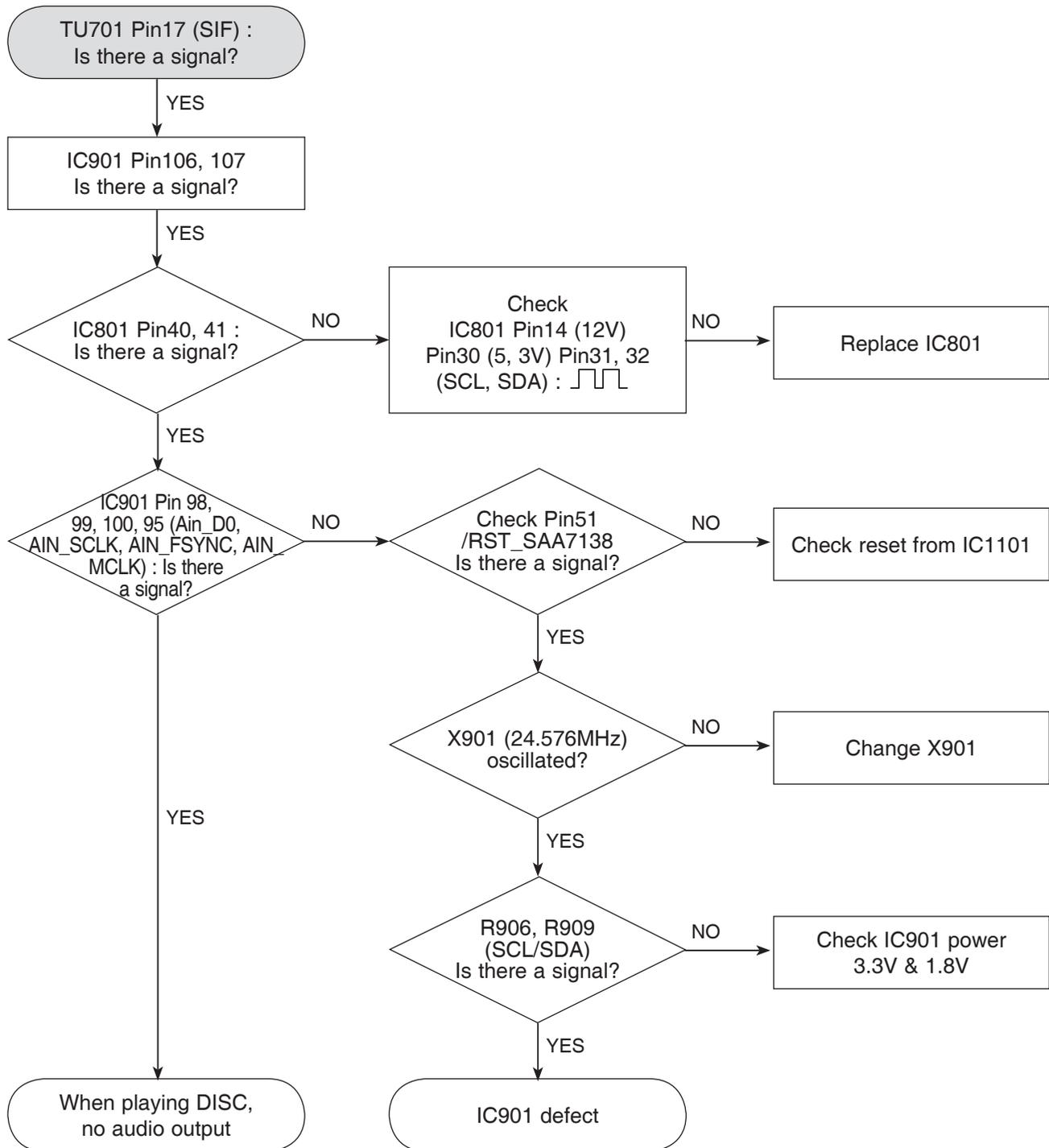
5. WHEN PLAYING DISC, NO AUDIO OUTPUT



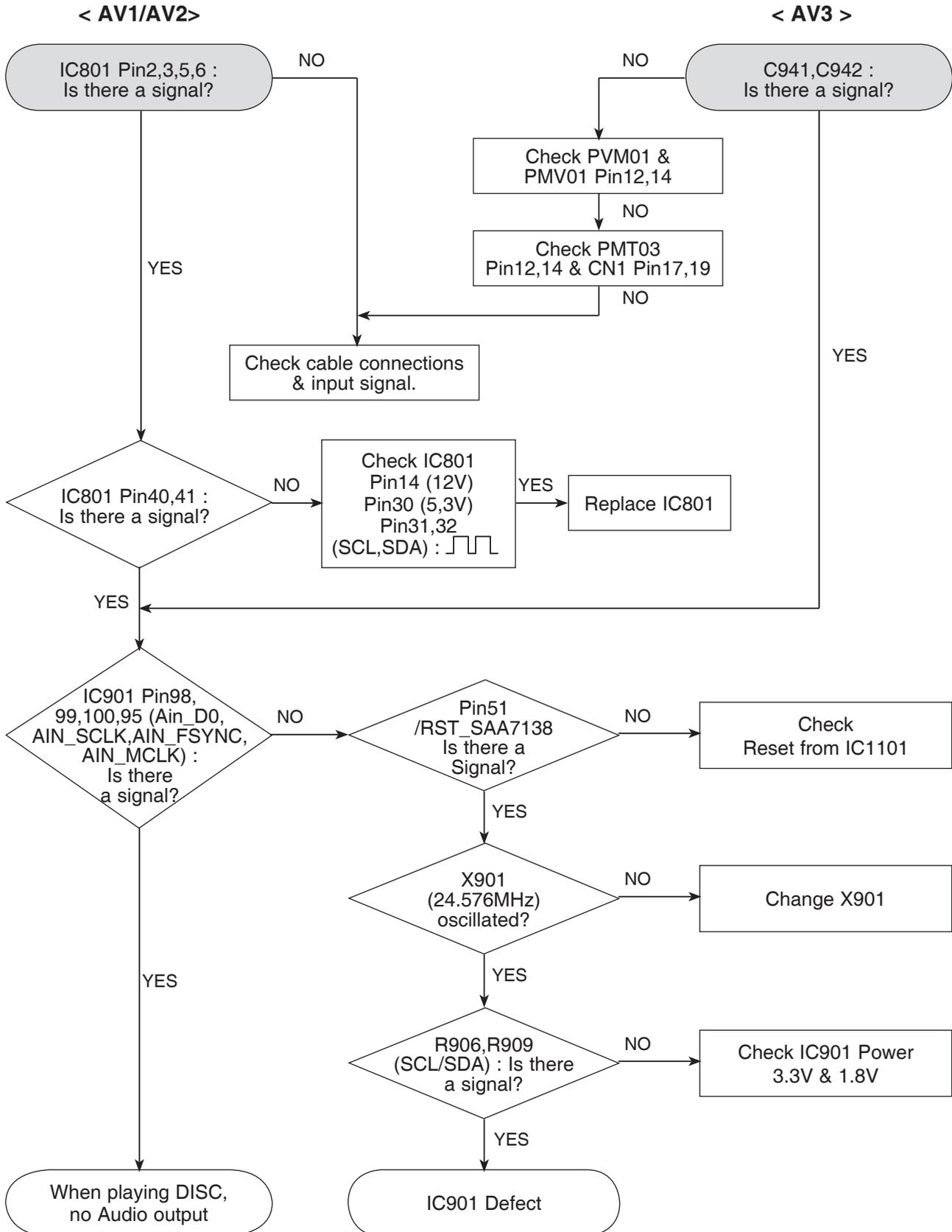
6. NO OPTICAL/DIGITAL OUTPUT



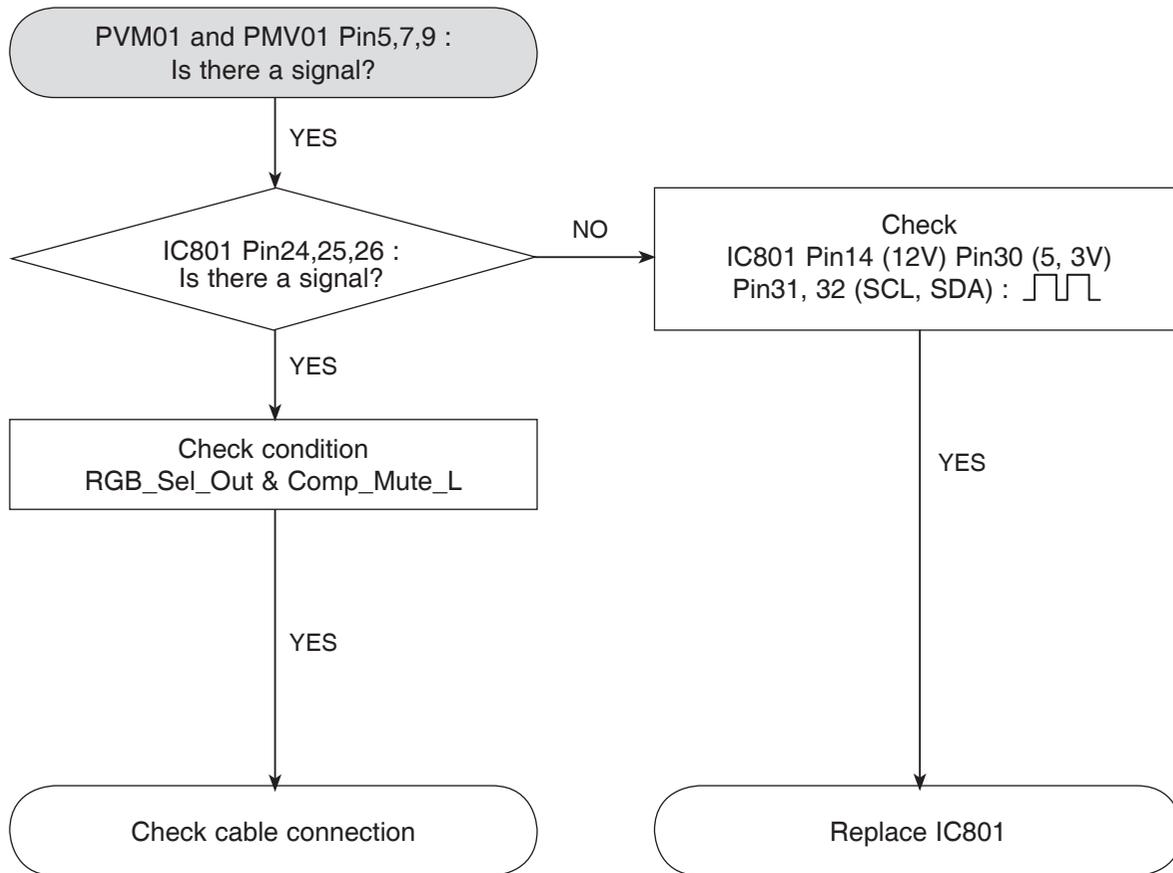
7. NO TUNER AUDIO OUTPUT



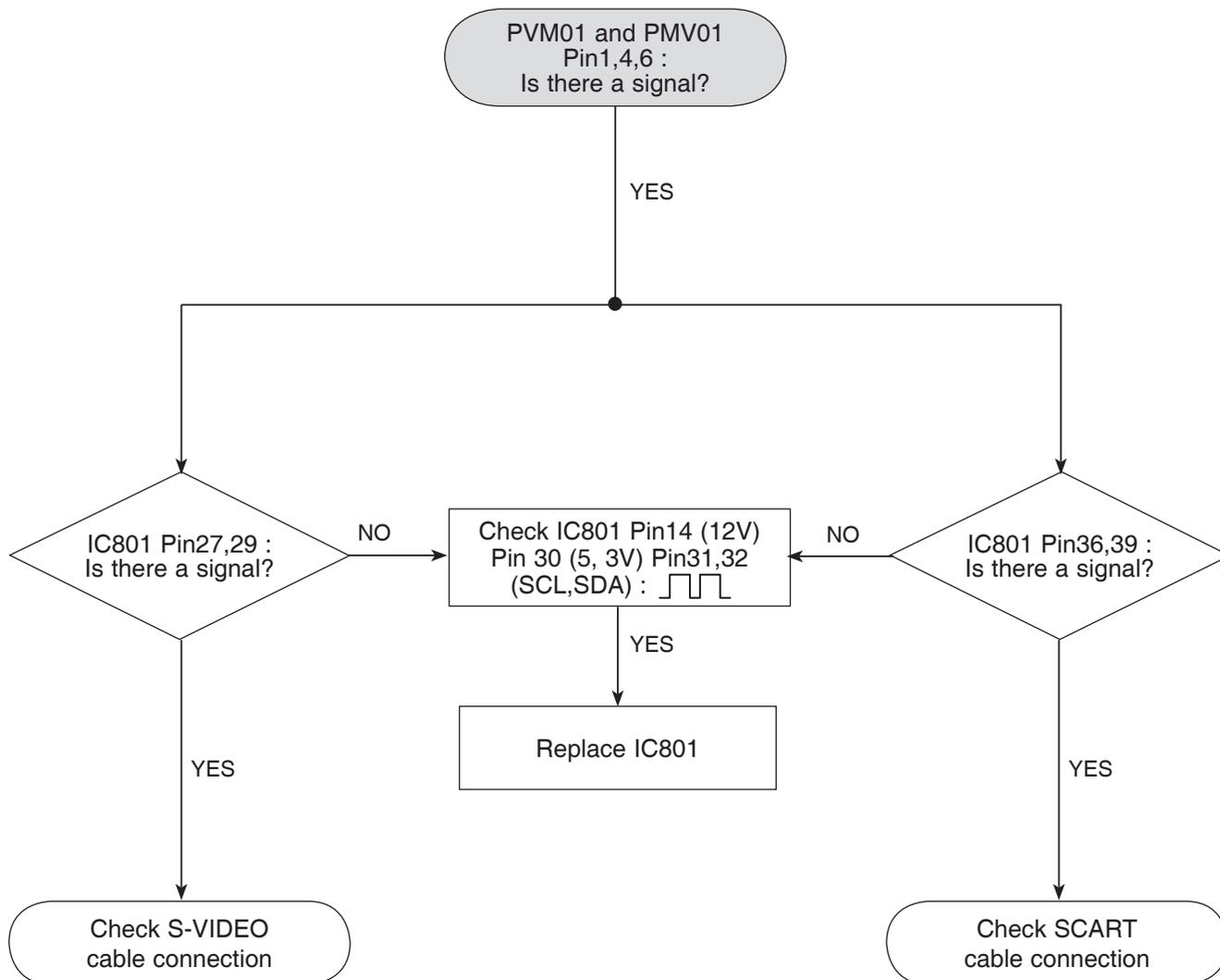
8. NO EXTERNAL AUDIO INPUT



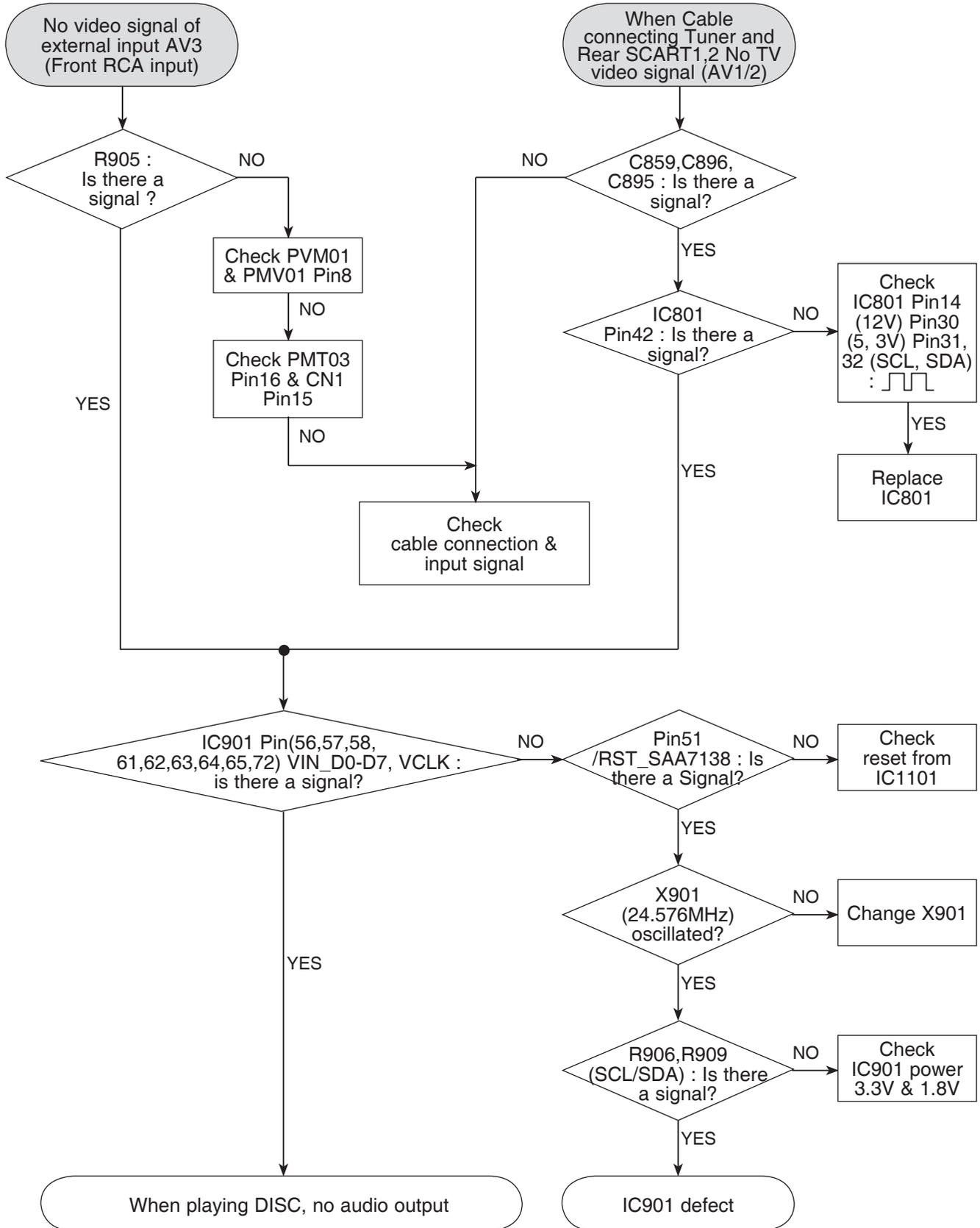
9. NO RGB / COMPONENT VIDEO SIGNAL WHEN PLAY DISC



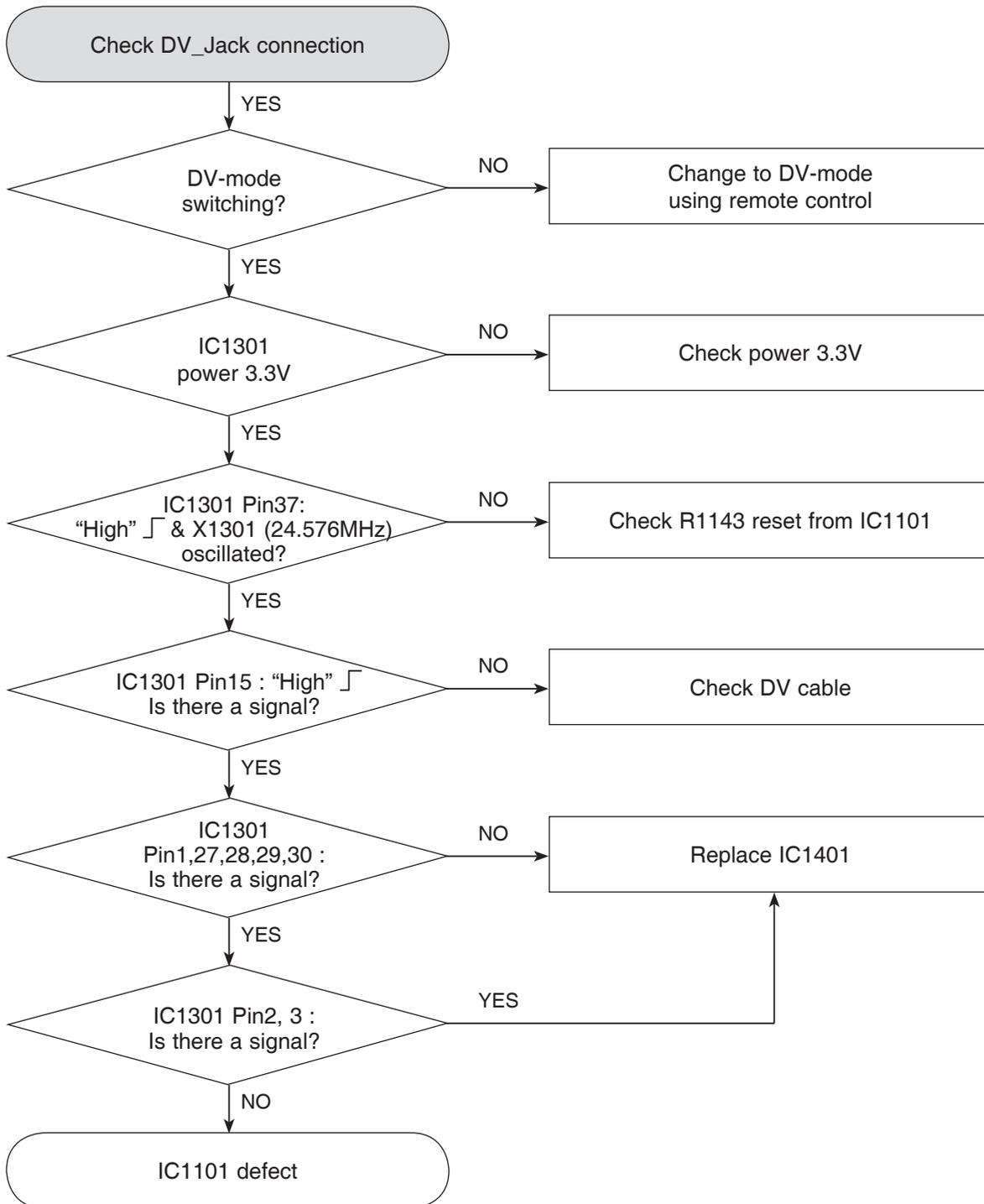
10. NO COMPOSITE / S-VIDEO SIGNAL WHEN PLAY DISC



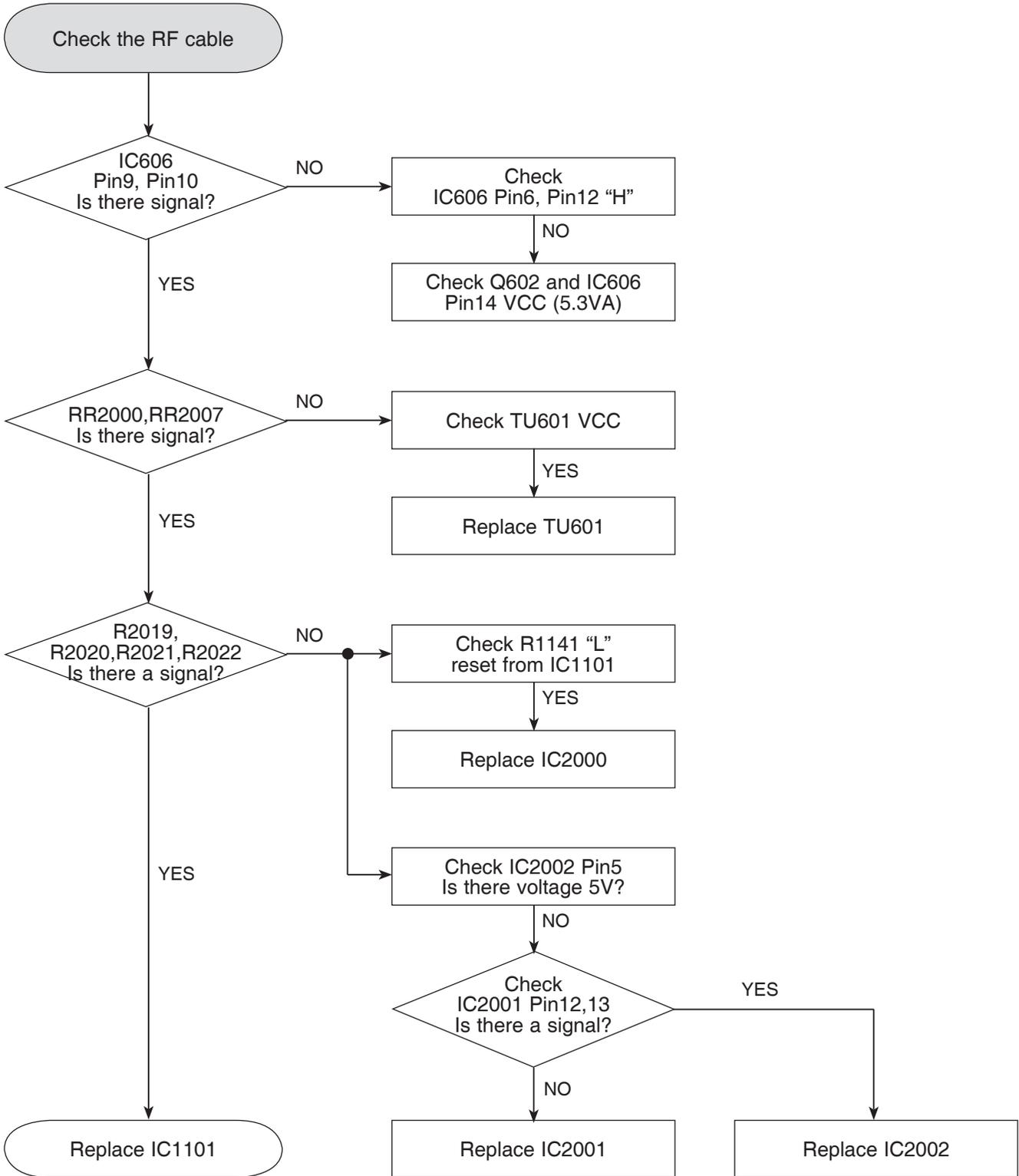
11. NO TV, EXTERNAL INPUT VIDEO SIGNAL

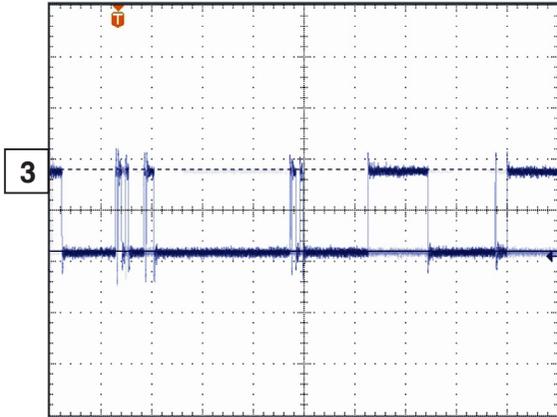


12. NO DV (IEEE1394) INPUT (VIDEO/AUDIO) SIGNAL

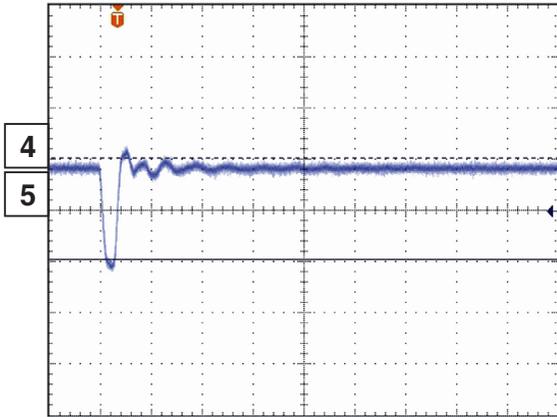


13. NO DVB_T AUDIO / VIDEO OUTPUT

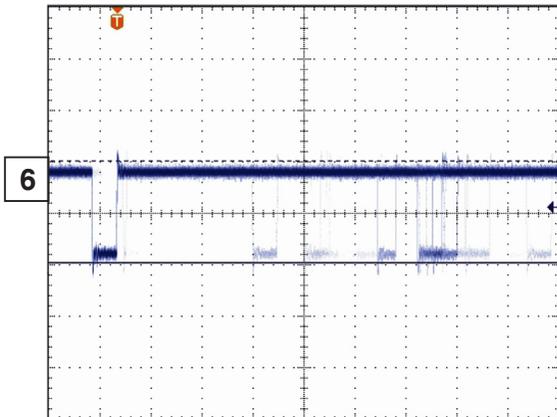




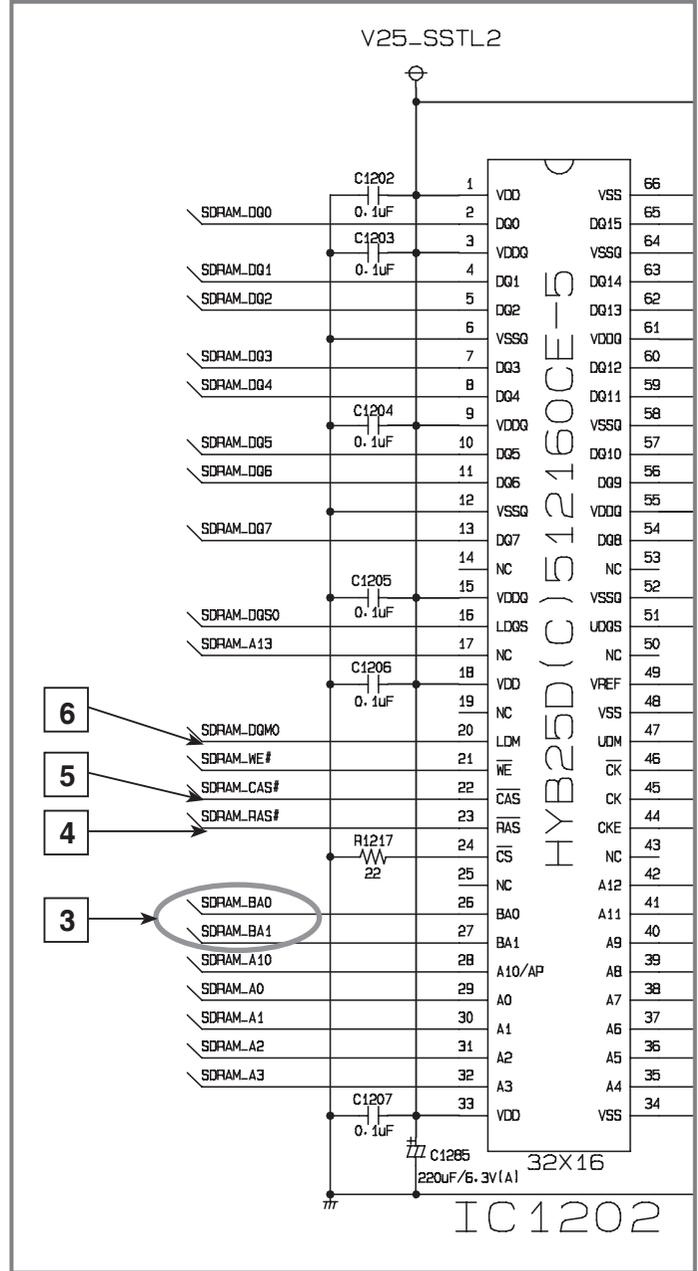
< DDR Bank Address >

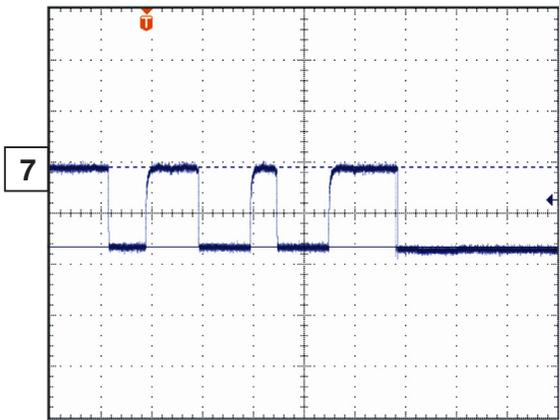
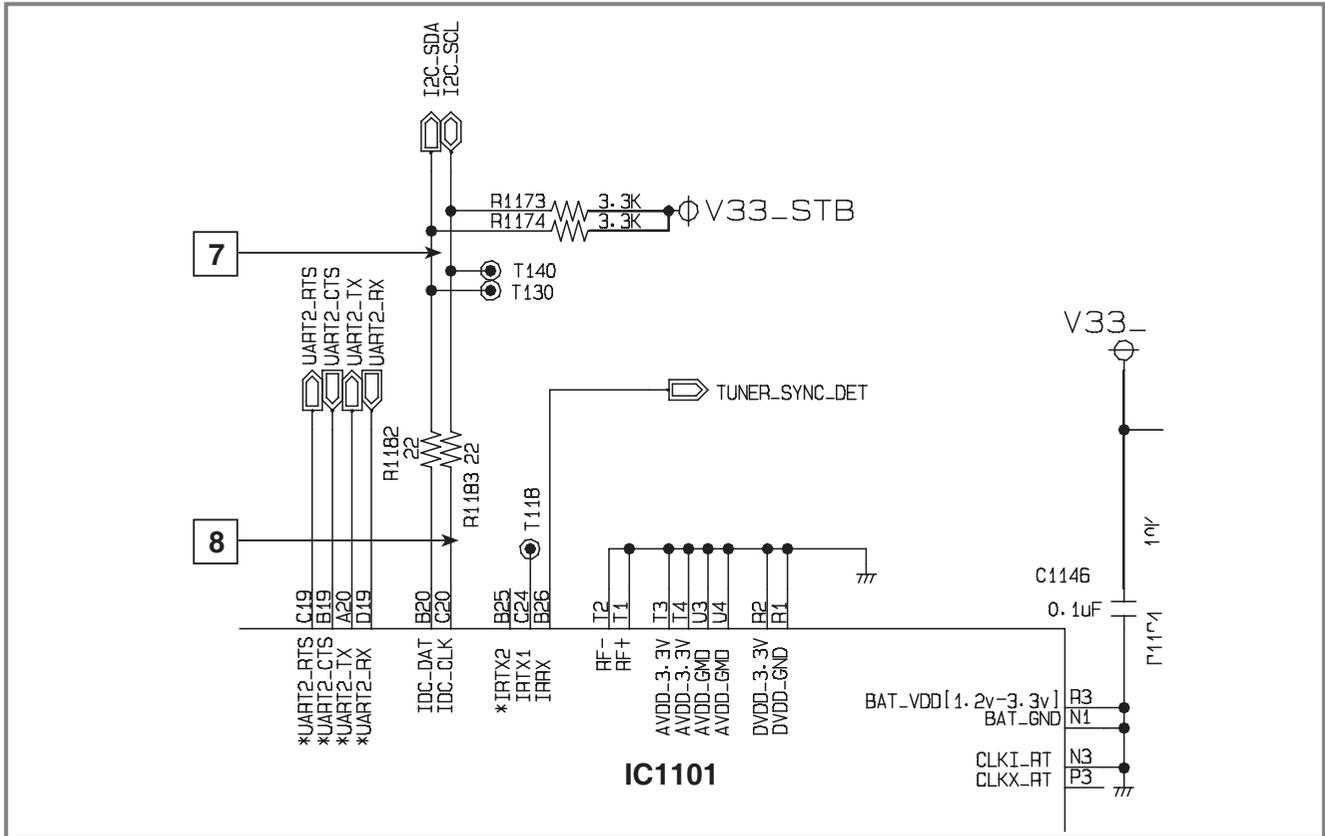


< DDR RAS & CAS >

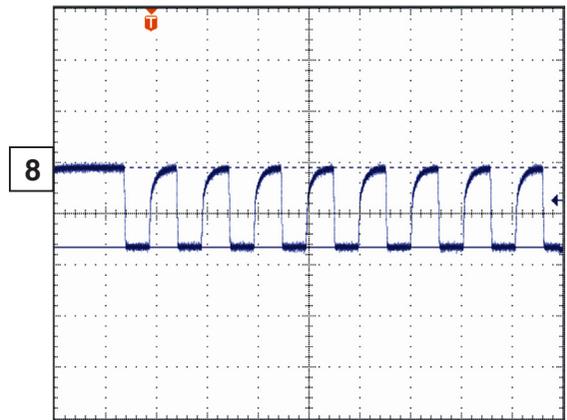


< DDR Write Enable >



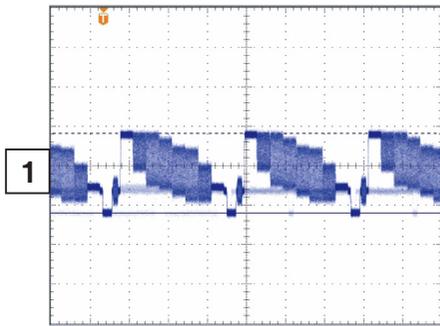


< 12C_SDA >

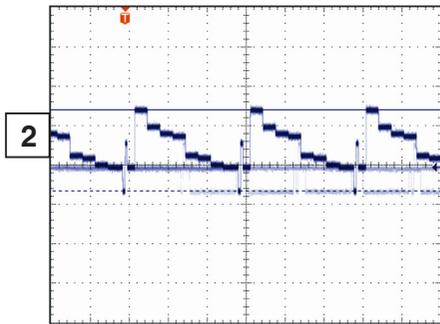


< 12C_SCL >

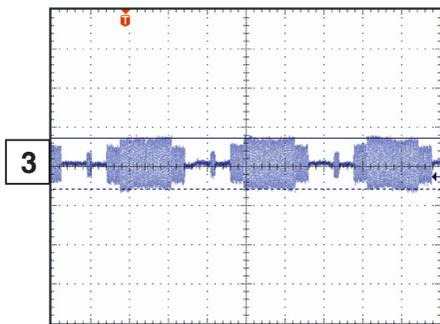
2. VIDEO BLOCK (COLOR BAR INPUT)



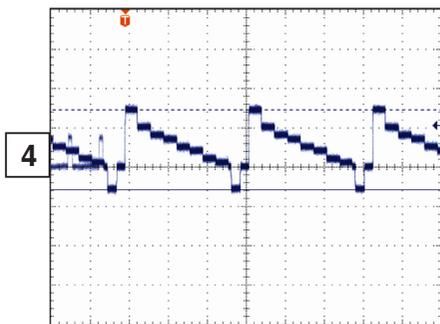
< CVBS_OUT >



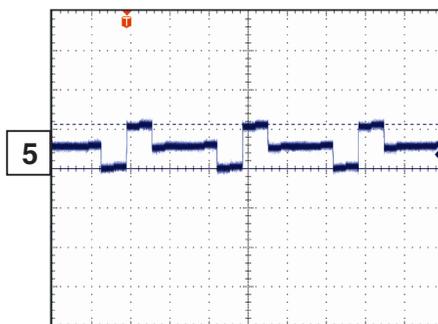
< Y_OUT >



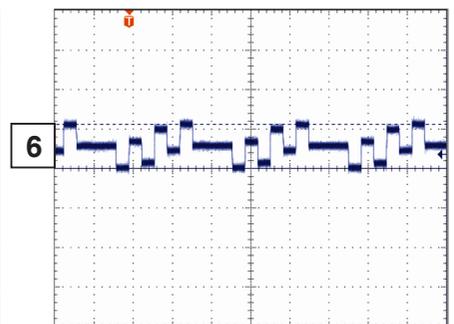
< C_OUT >



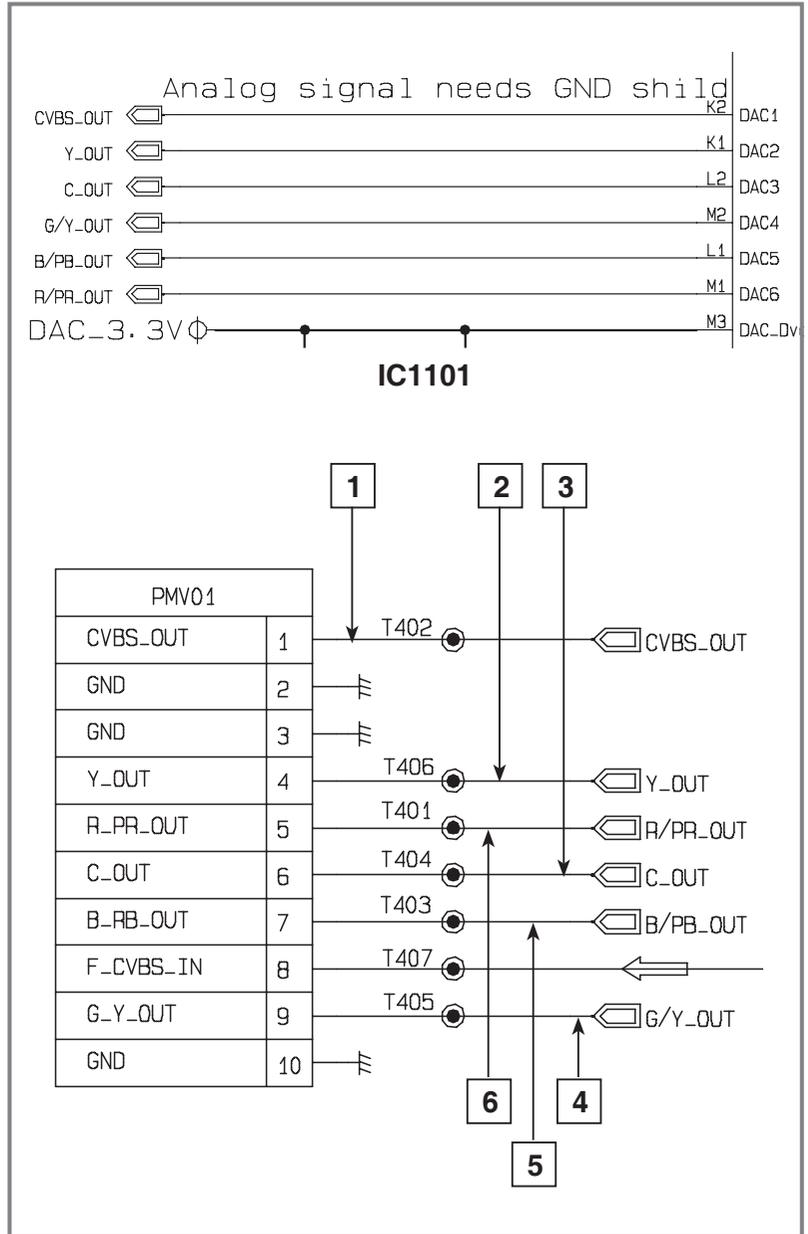
< G/Y_OUT >



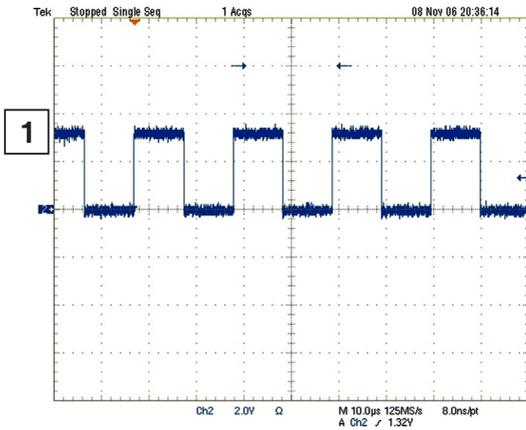
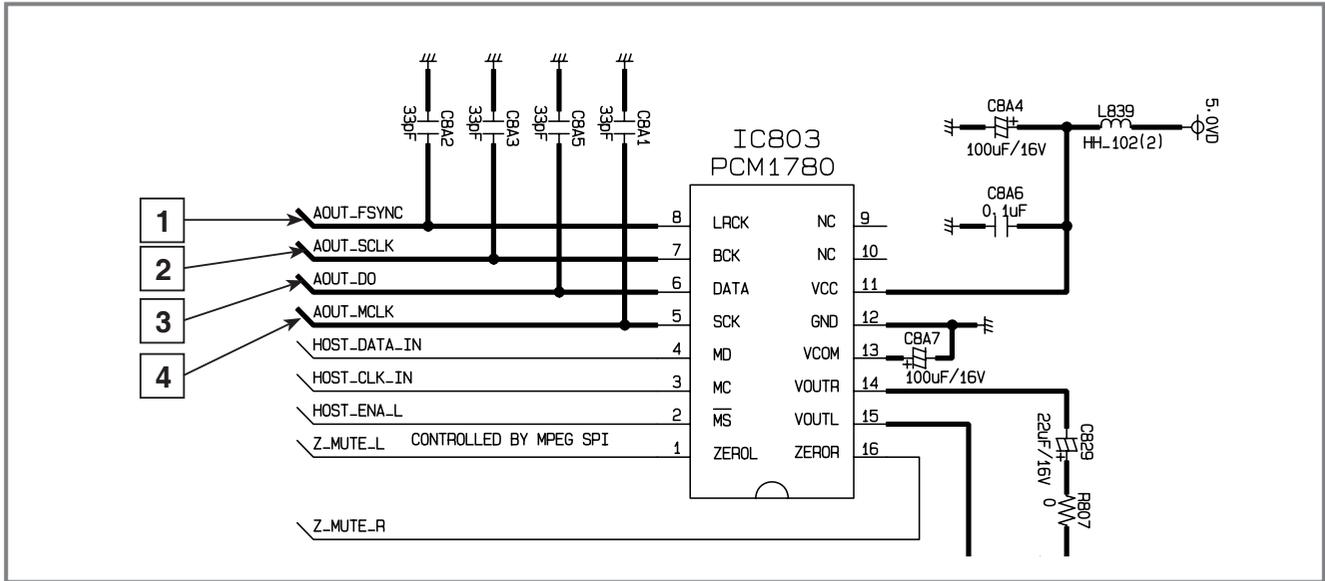
< B/PB_OUT >



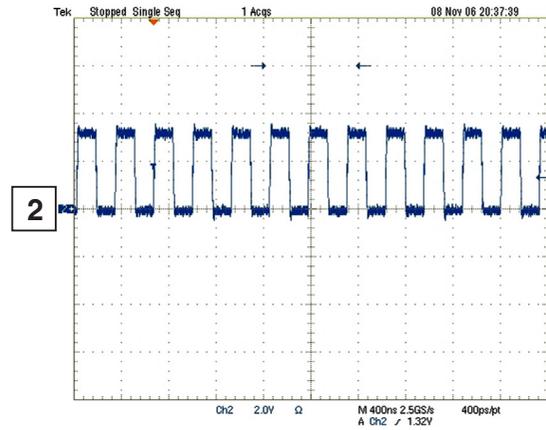
< R/PR_OUT >



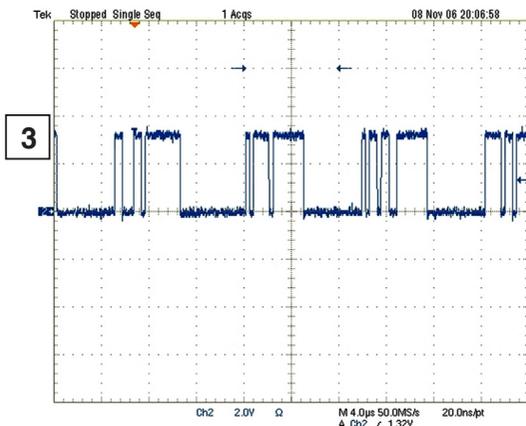
3. AUDIO BLOCK (1kHz SINEWAVE INPUT)



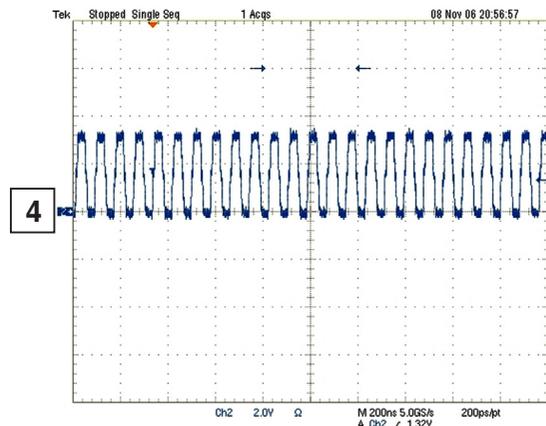
< AOUT_FSYNC >



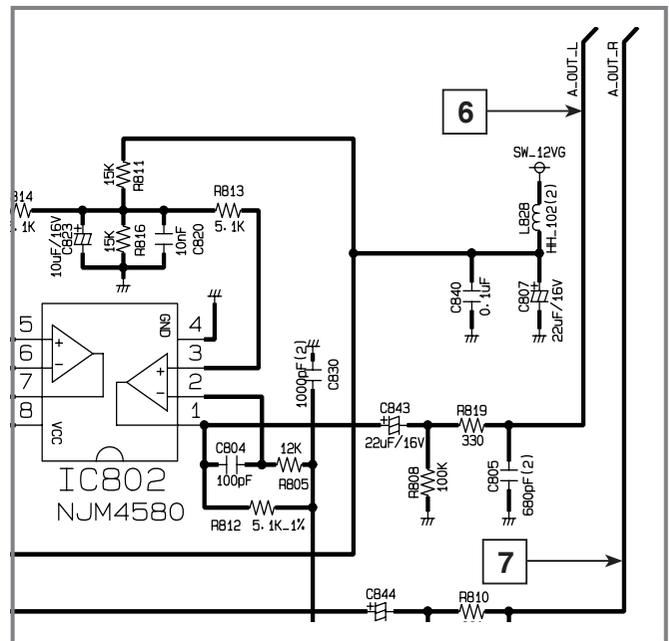
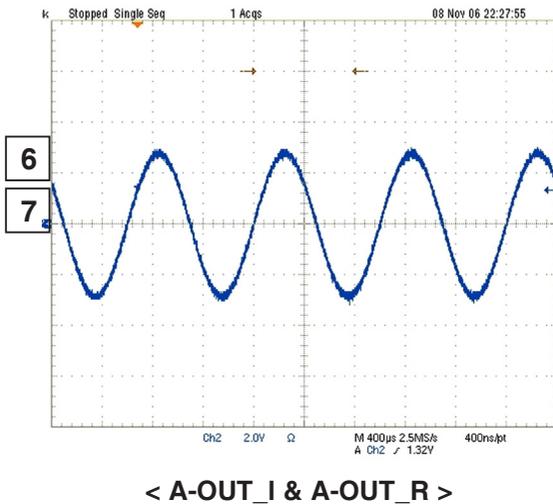
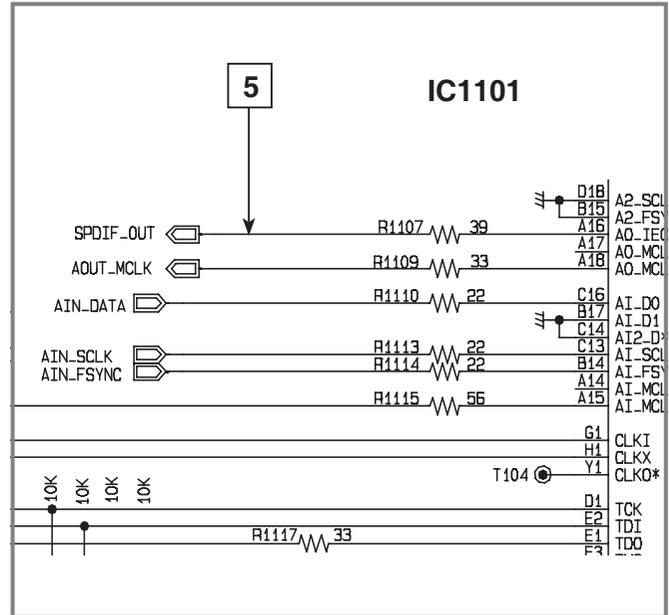
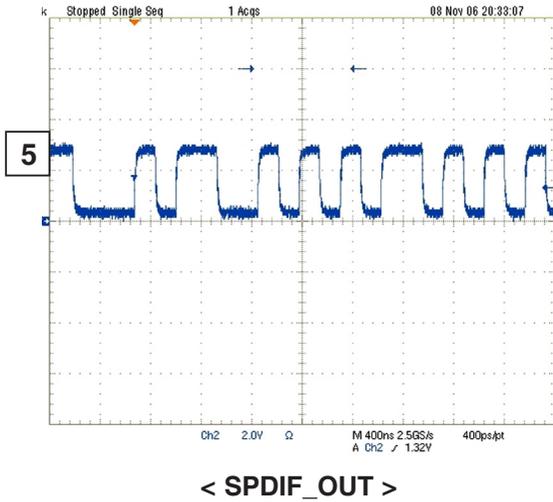
< AOUT_SCLK >



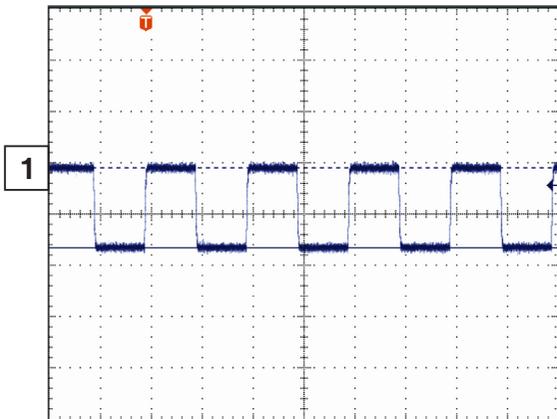
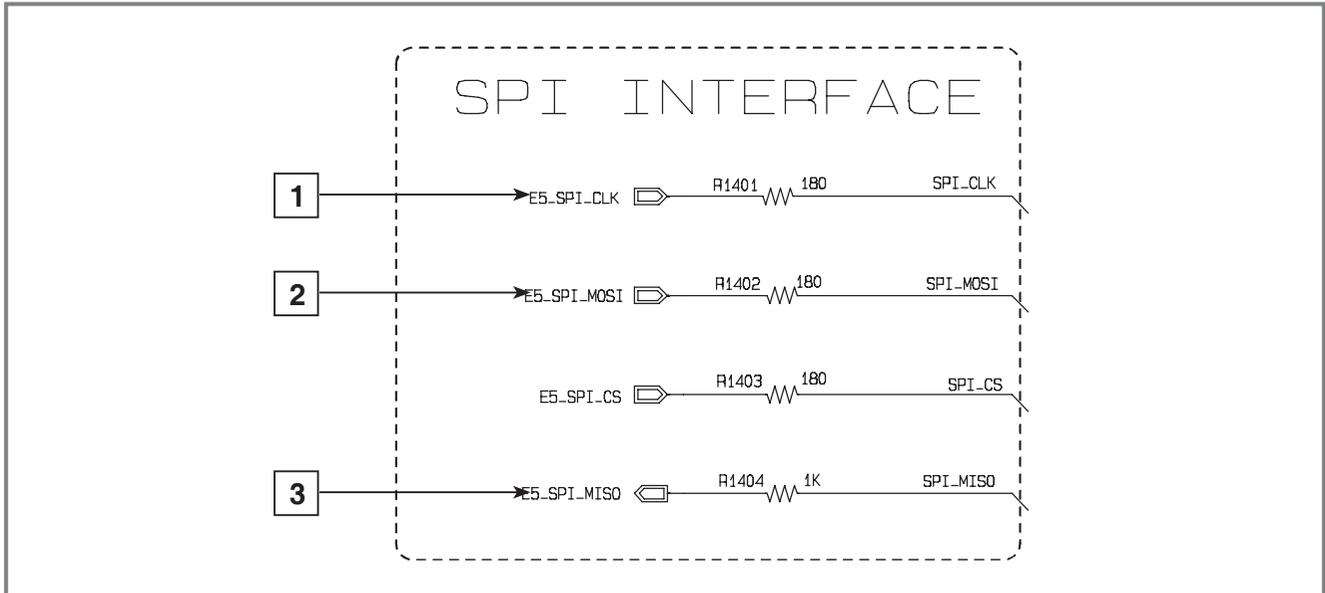
< AOUT_DO >



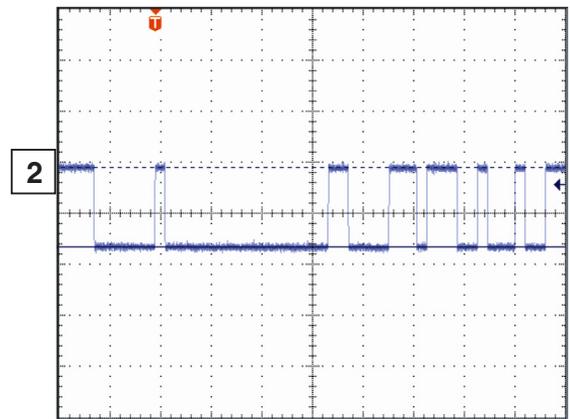
< AOUT_MCLK >



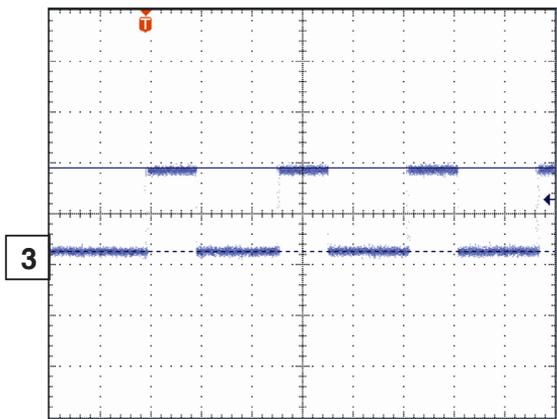
4. SERIAL INTERFACE BLOCK (BETWEEN MAIN & I/O)



< E5_SPI_CLK >

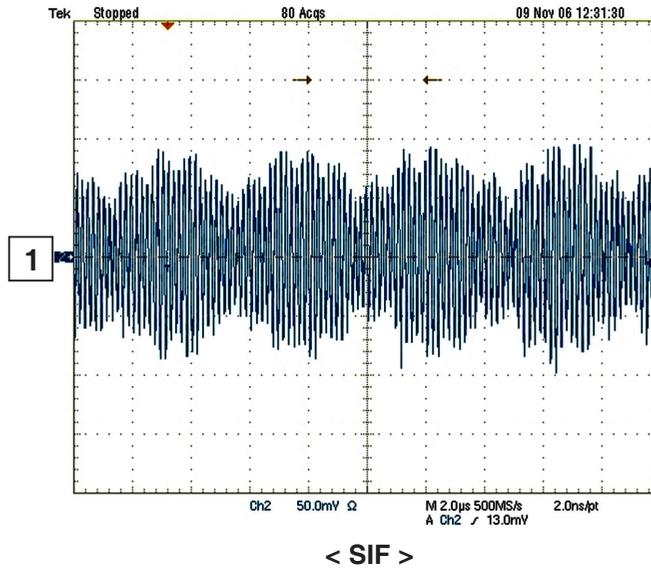
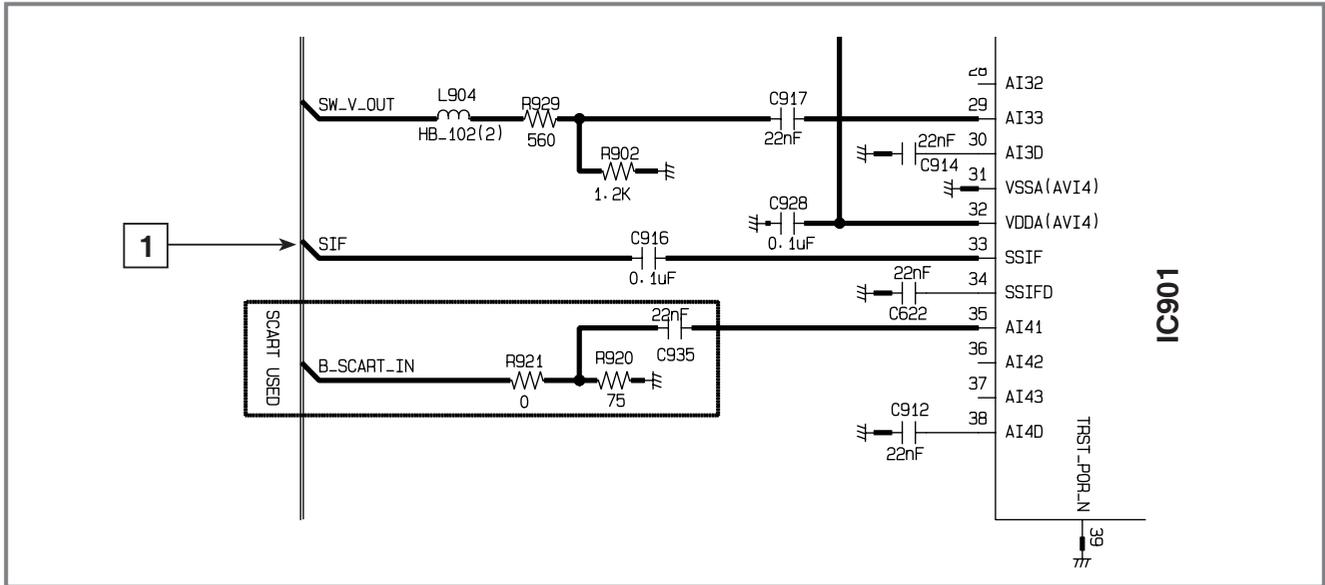


< E5_SPI_MOSI >

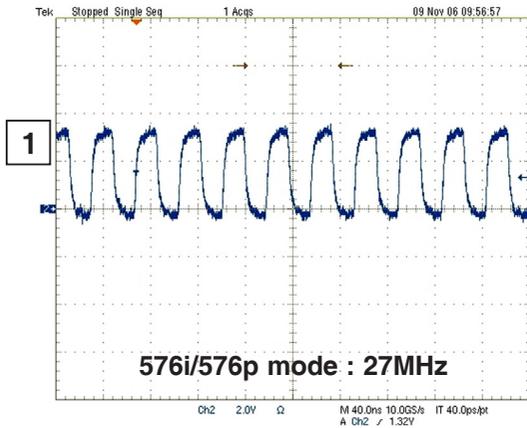
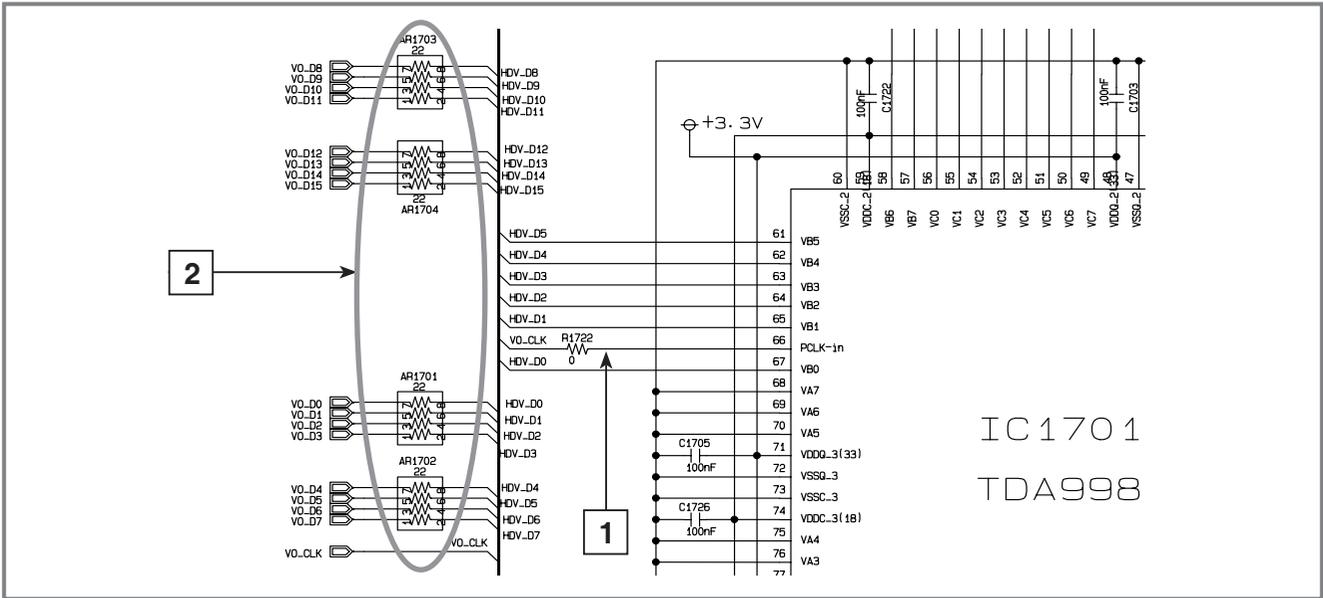


< E5_SPI_MISO >

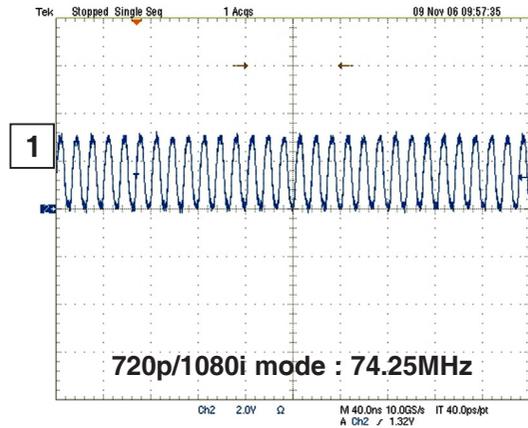
5. TUNER BLOCK



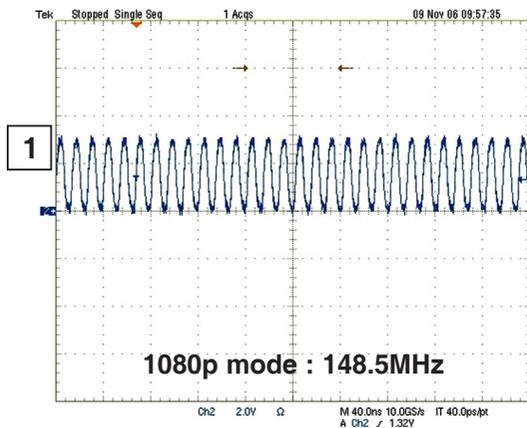
6. HDMI BLOCK



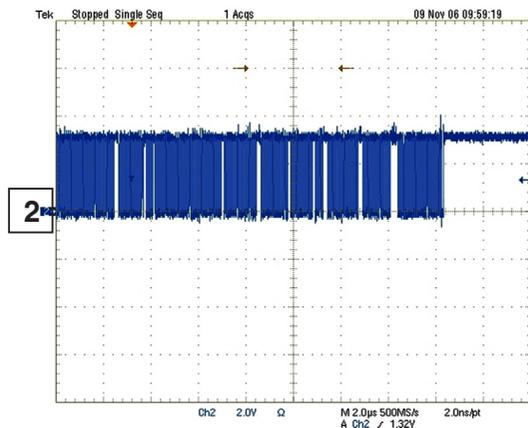
< VOUT_CLK >



< VOUT_CLK >



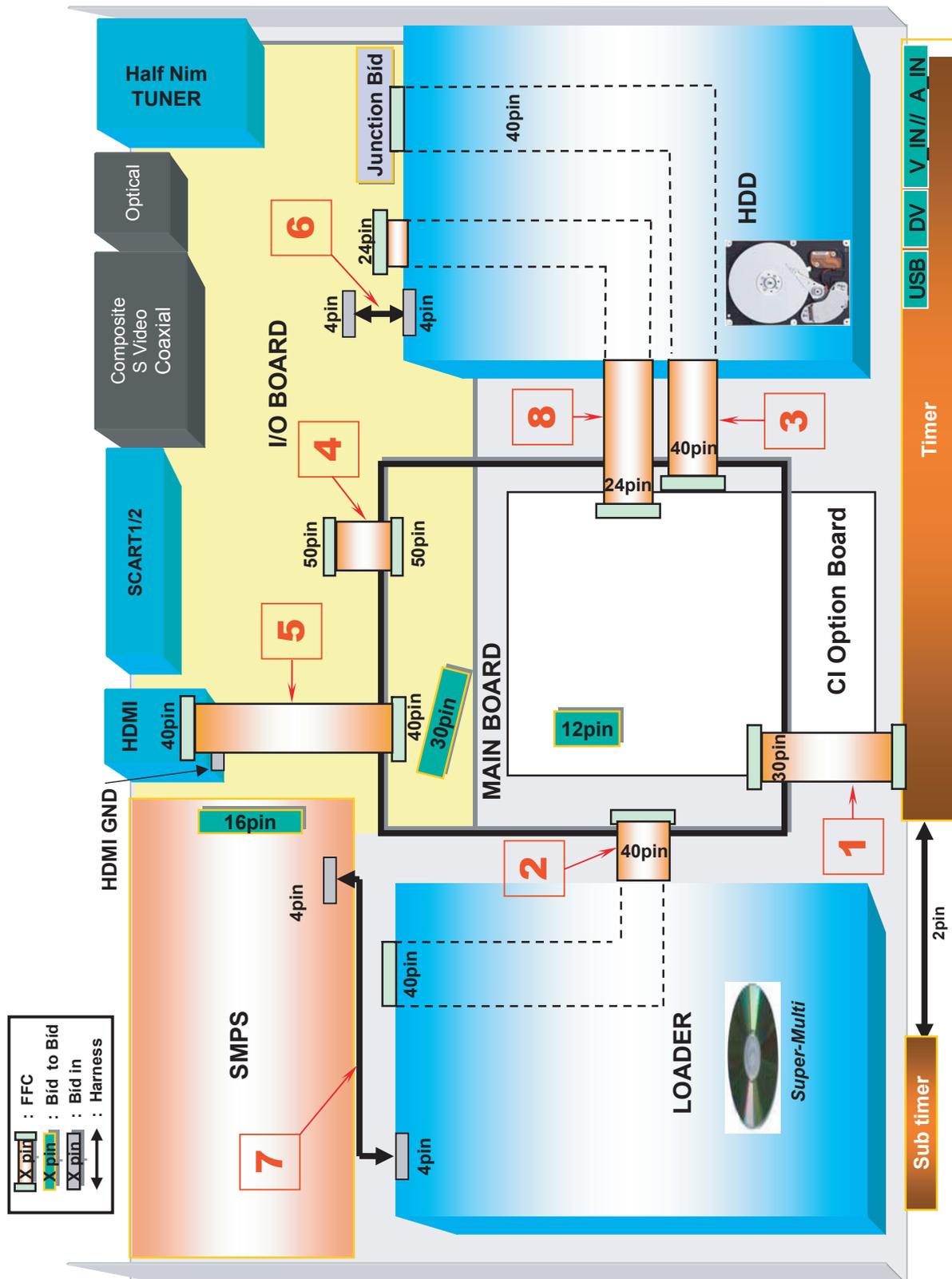
< VOUT_CLK >



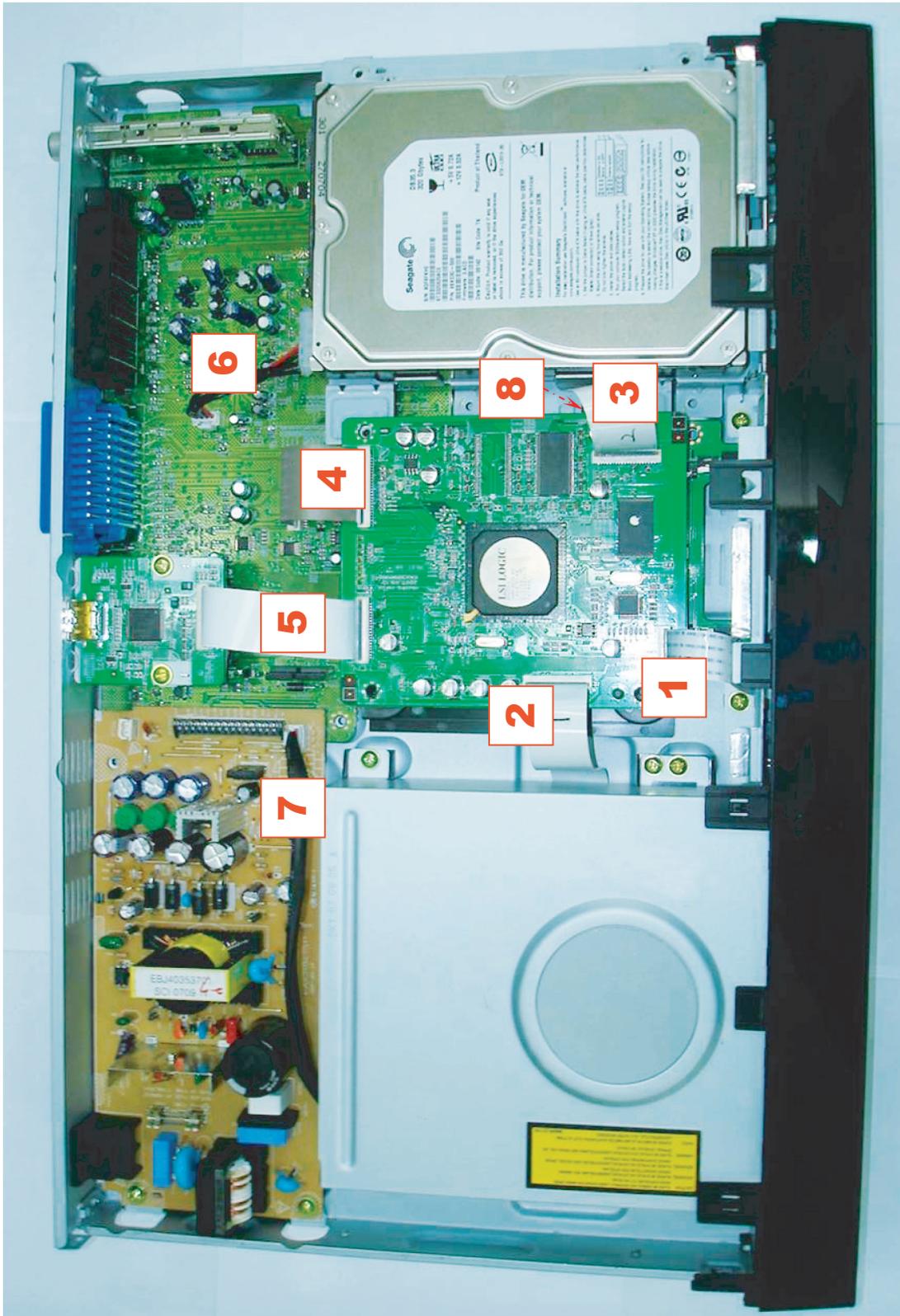
< AOUT_MCLK >

WIRING DIAGRAMS

1. WIRING DIAGRAM 1



2. WIRING DIAGRAM 2



1



2



3



4



5



6



7

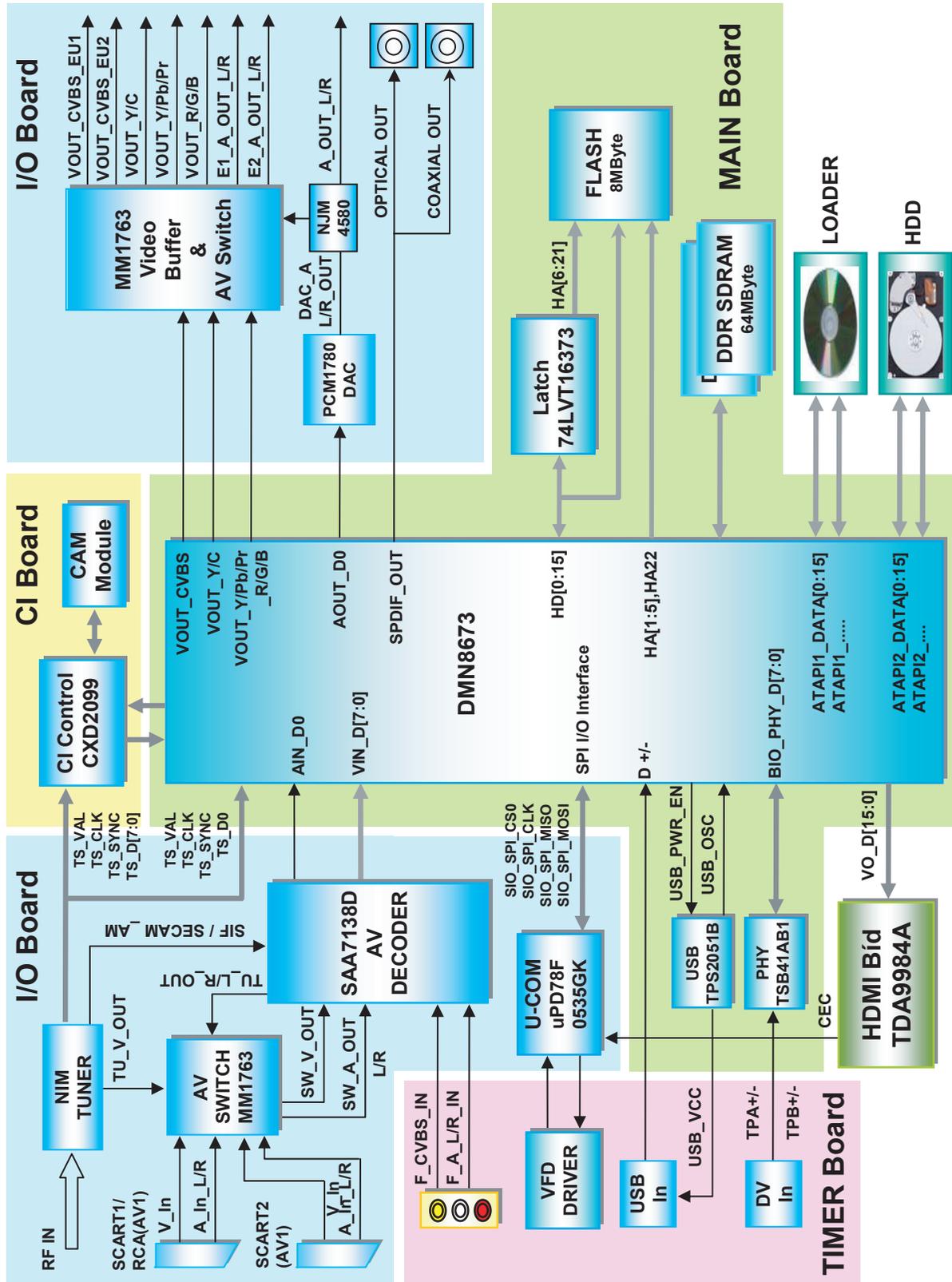


8
Option

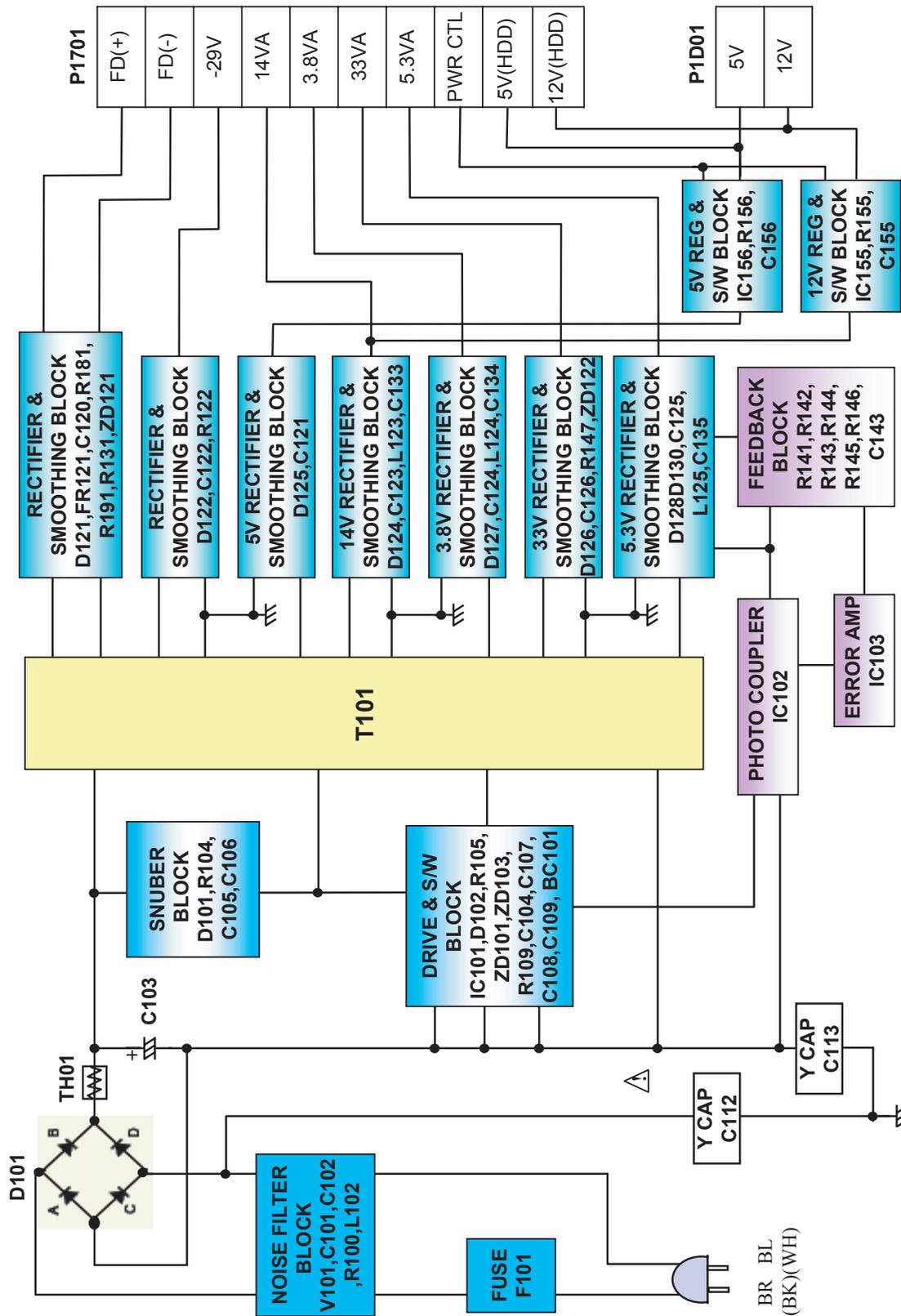


BLOCK DIAGRAMS

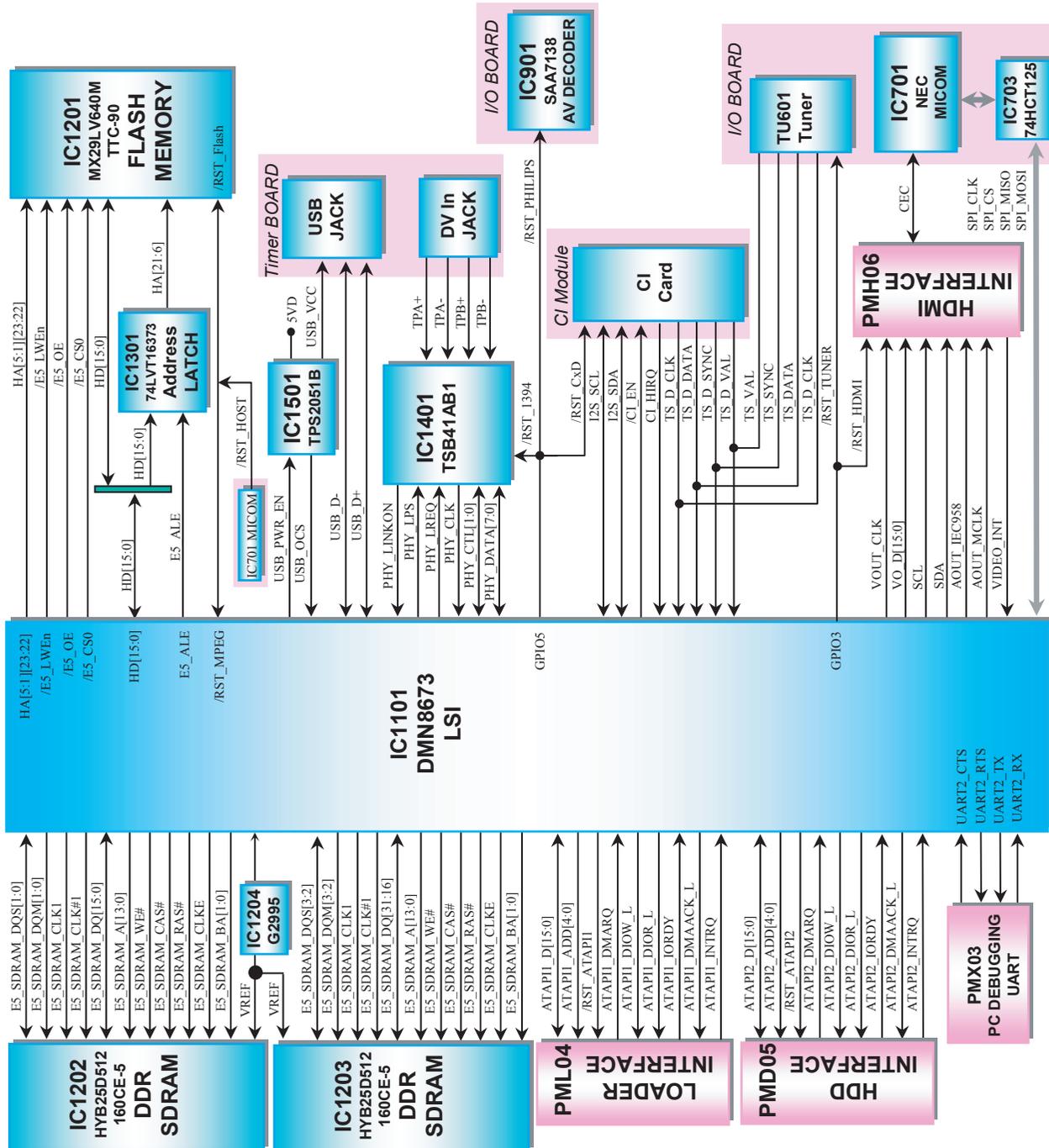
1. OVERALL BLOCK DIAGRAM



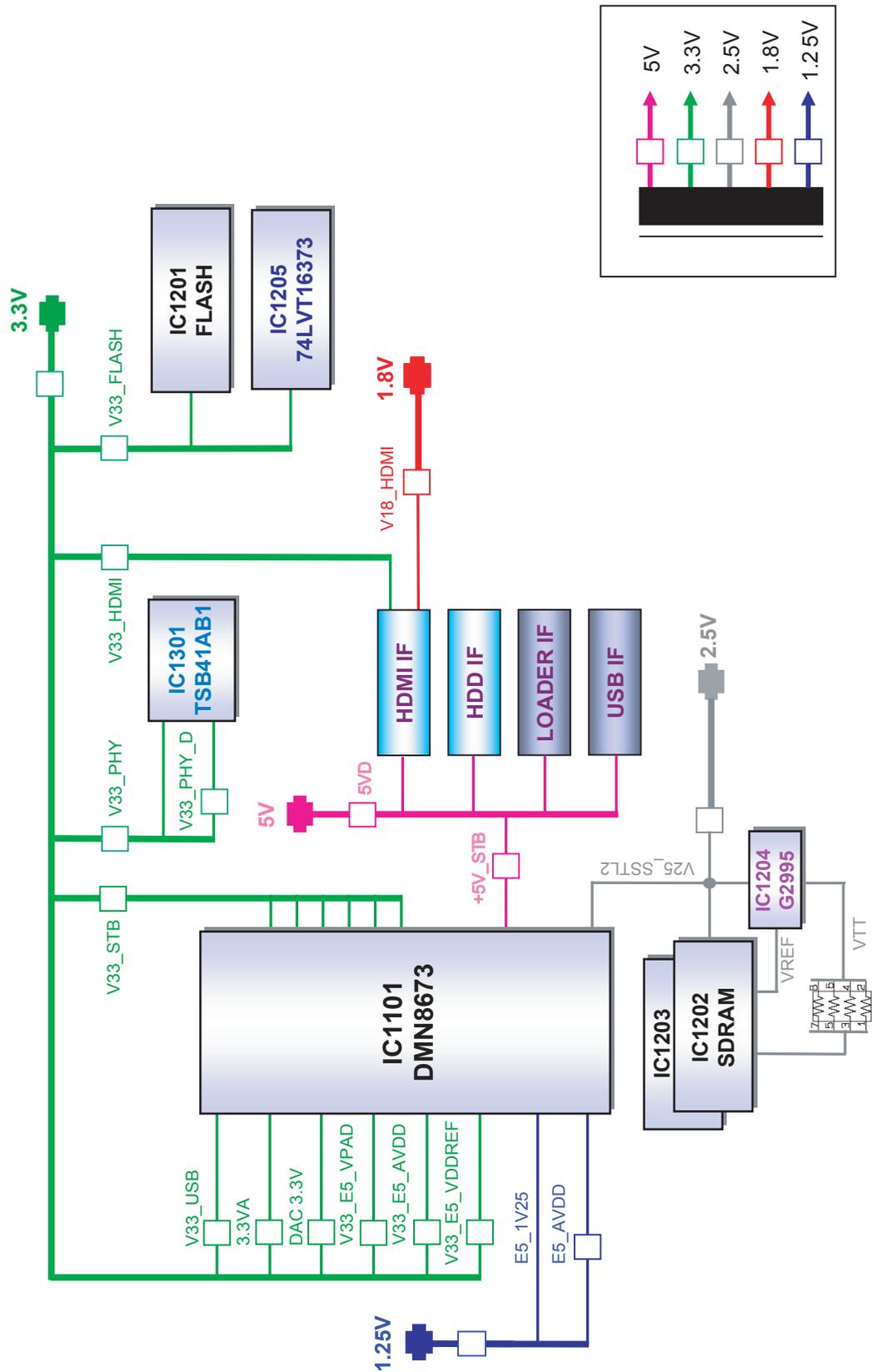
2. SMPS BOARD BLOCK DIAGRAM



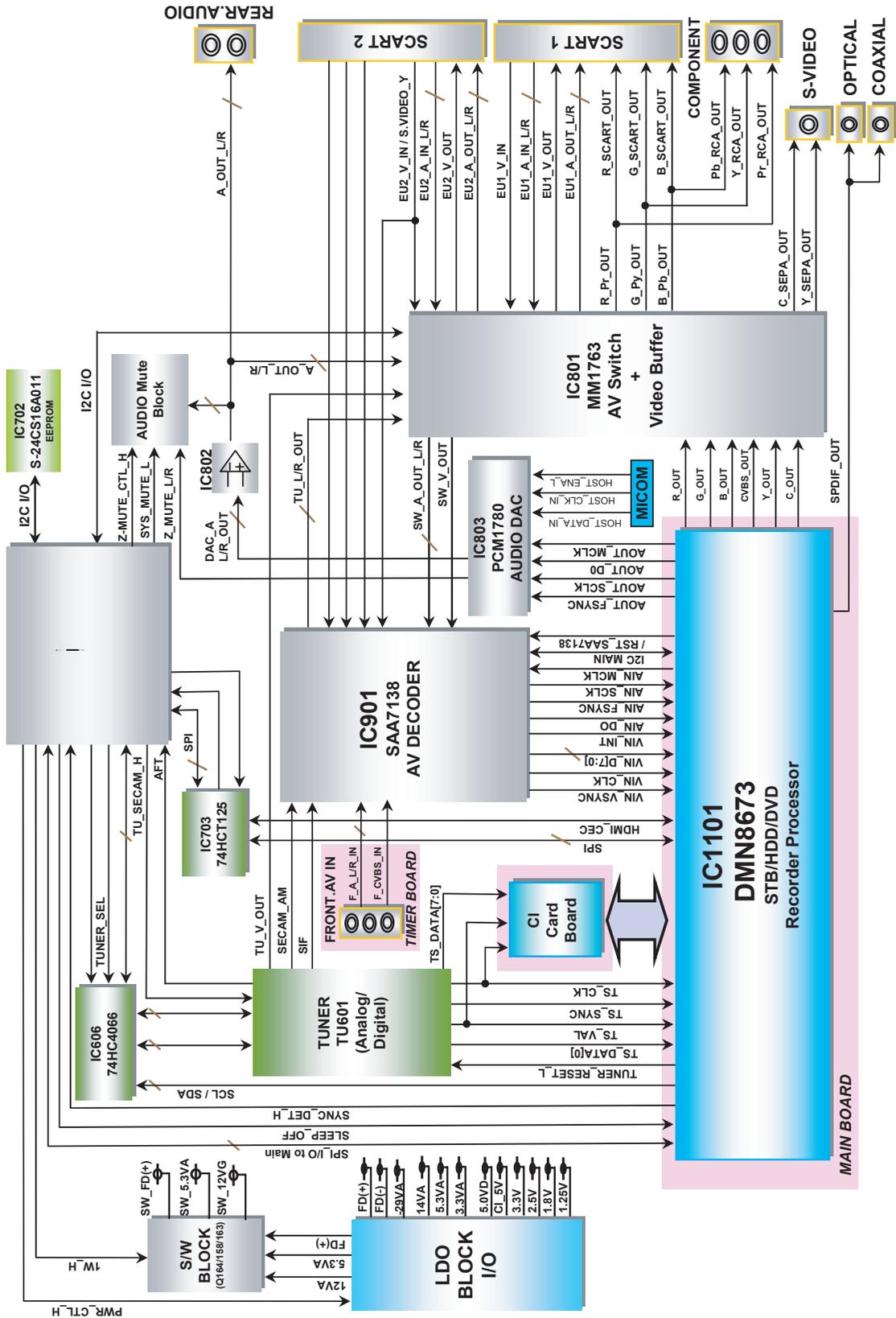
3. MAIN BOARD BLOCK DIAGRAM



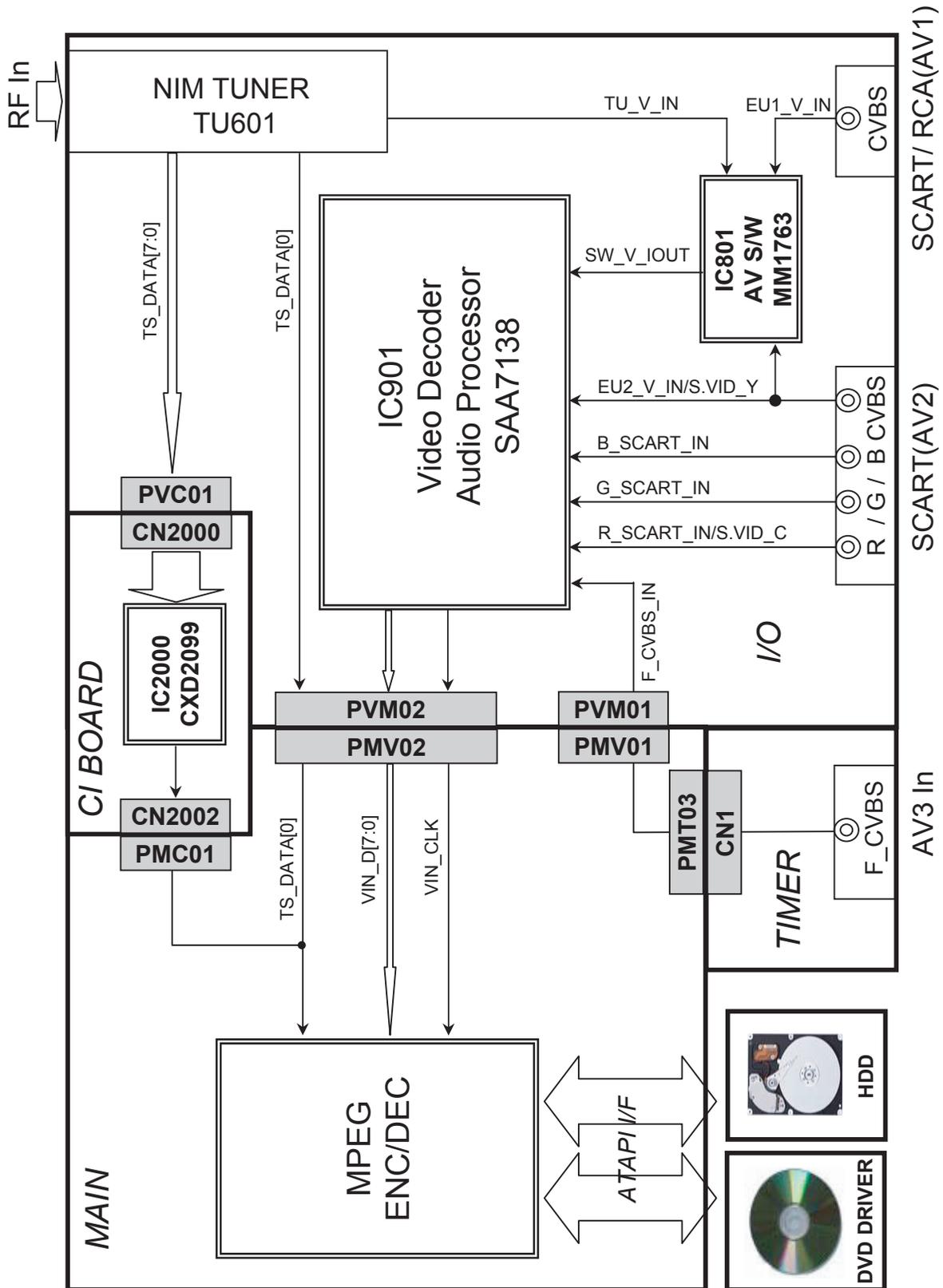
4. POWER MAIN BOARD BLOCK DIAGRAM



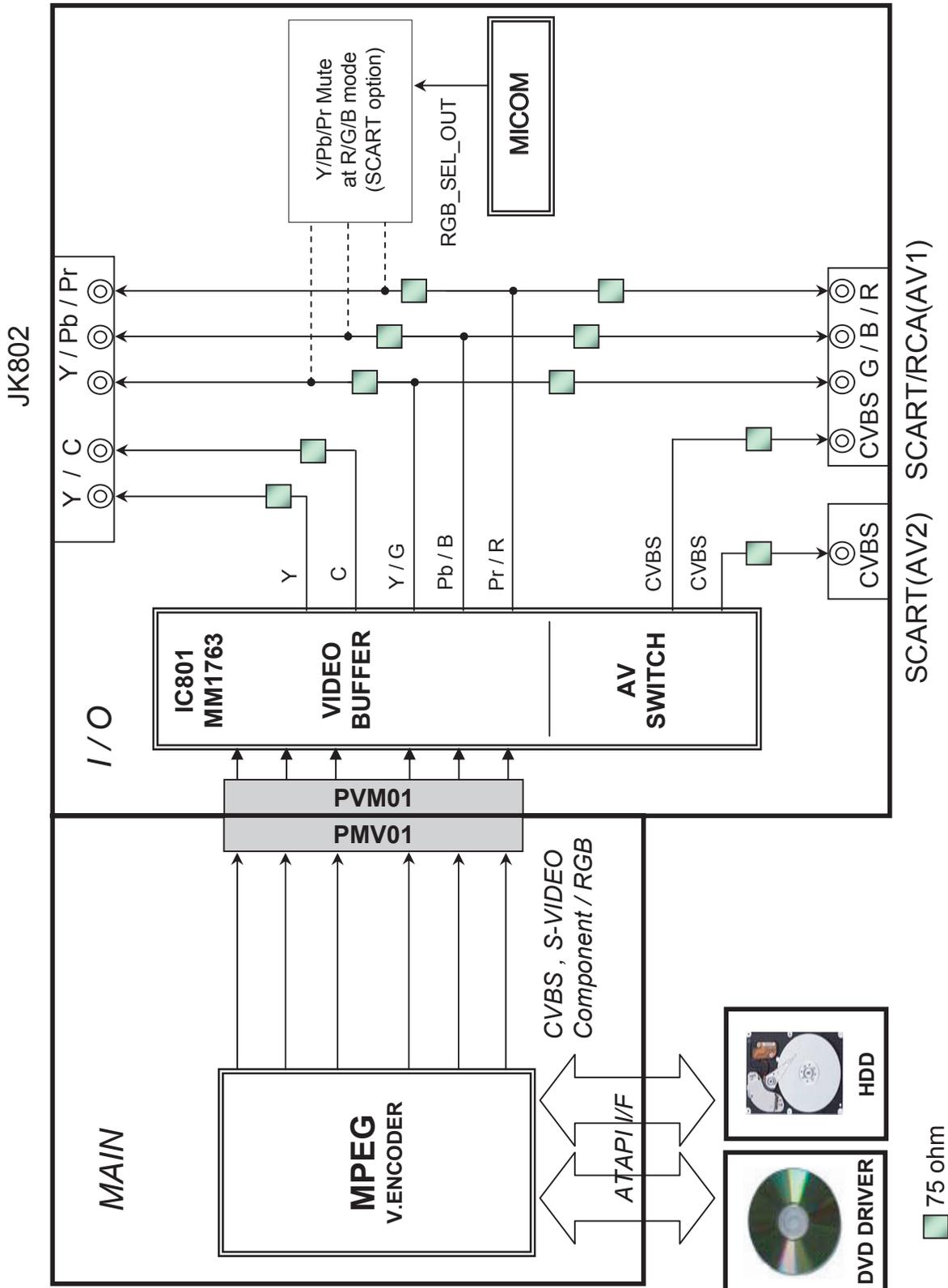
5. I/O BOARD BLOCK DIAGRAM



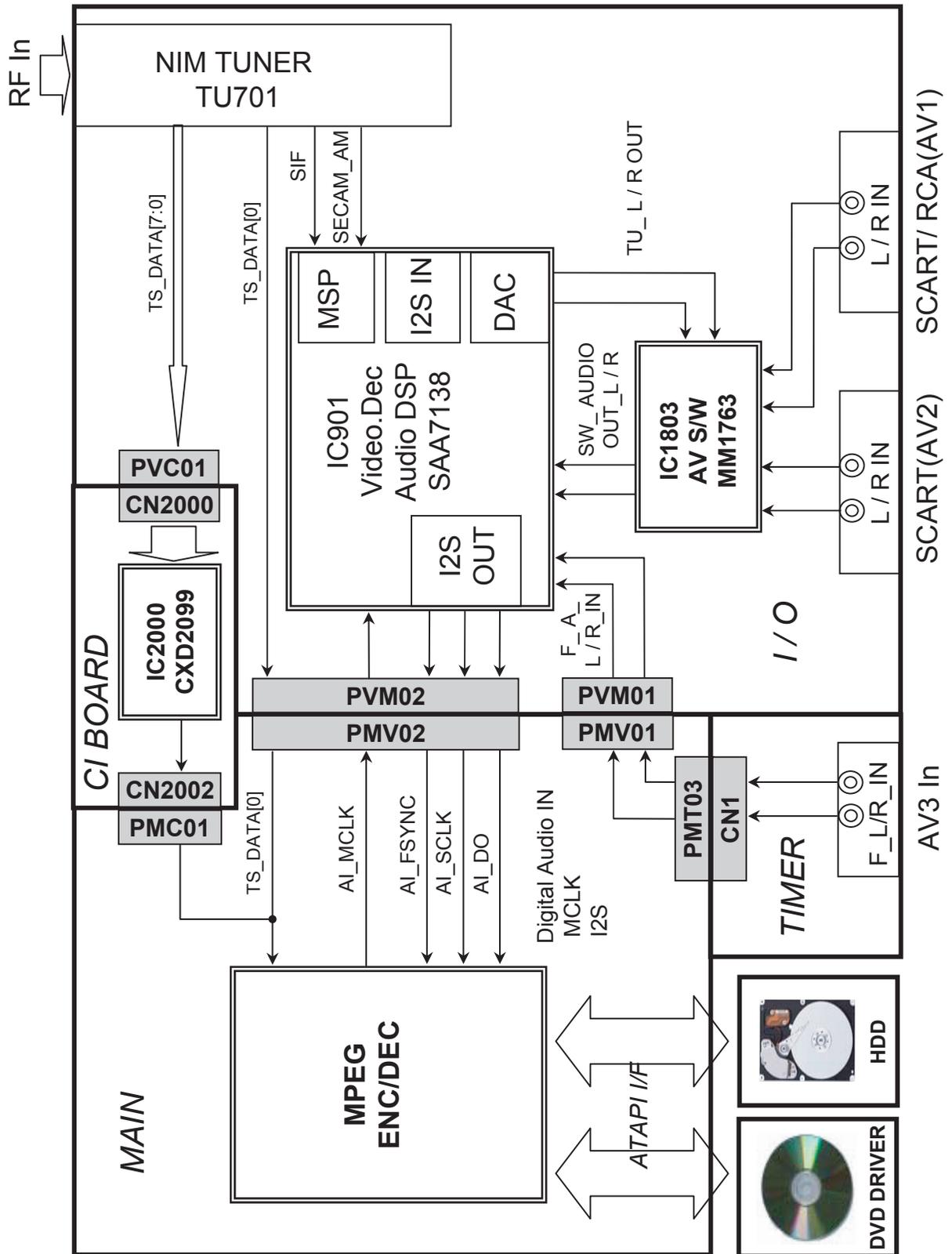
6. VIDEO INPUT BLOCK DIAGRAM



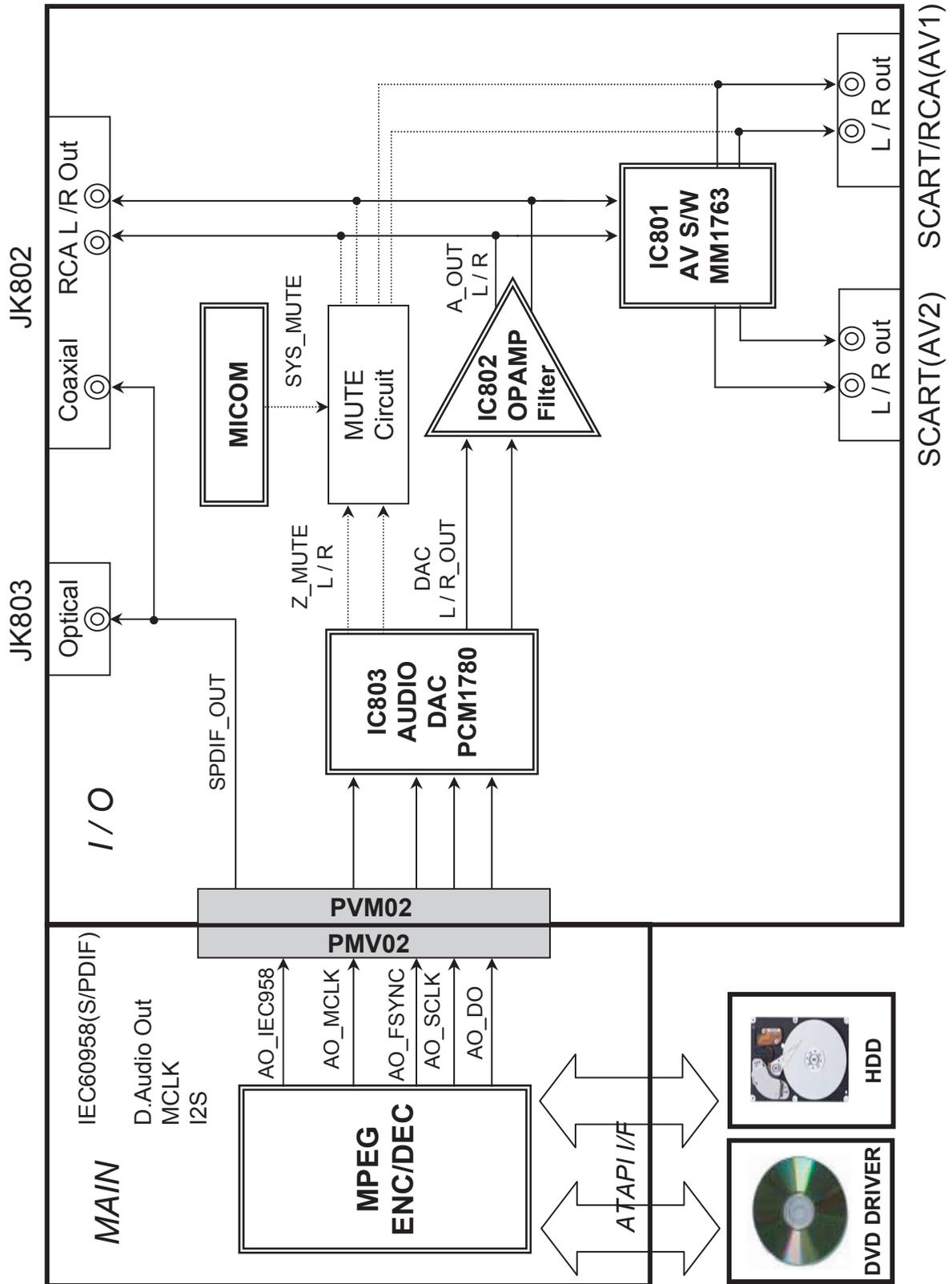
7. VIDEO OUTPUT BLOCK DIAGRAM



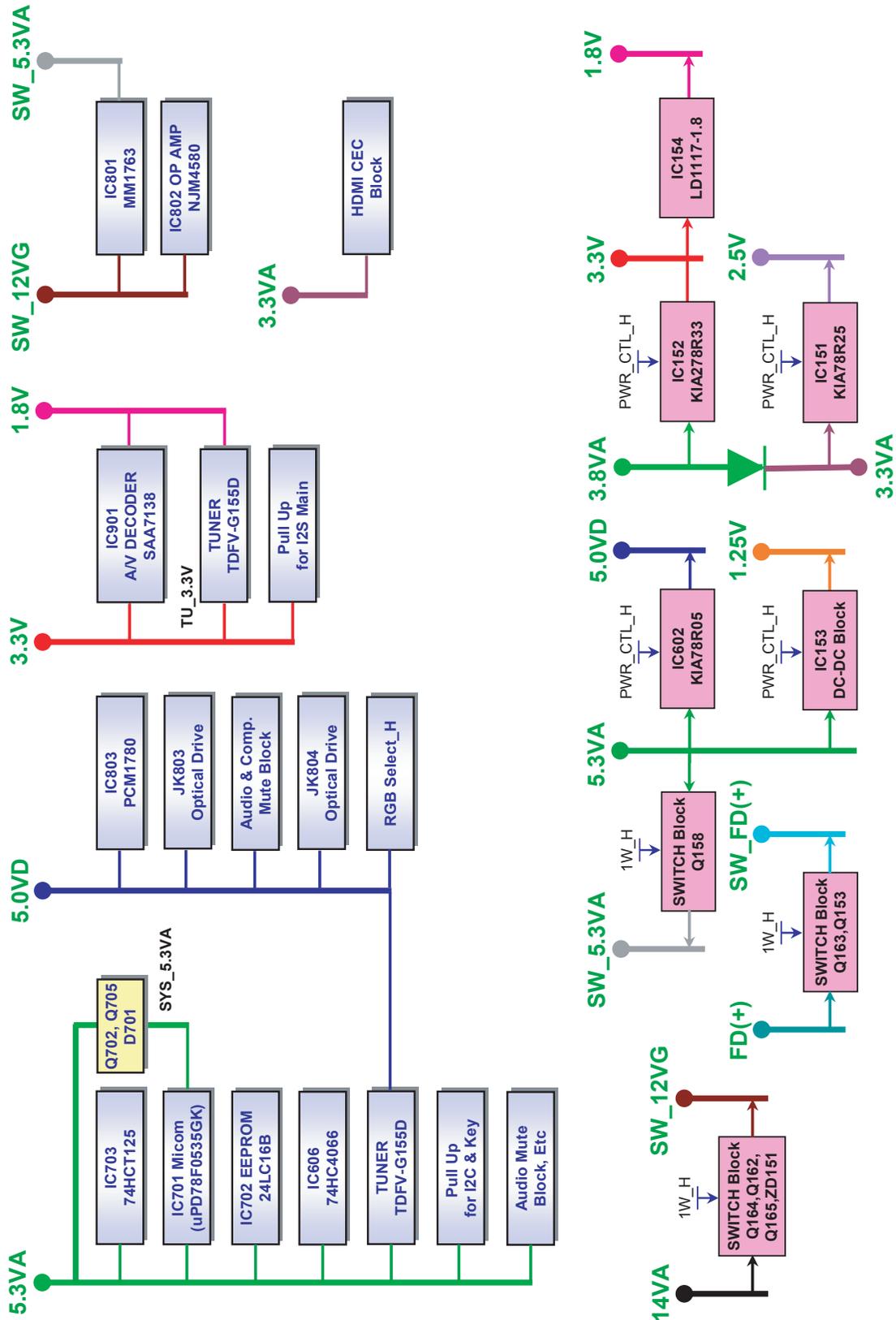
8. AUDIO INPUT BLOCK DIAGRAM



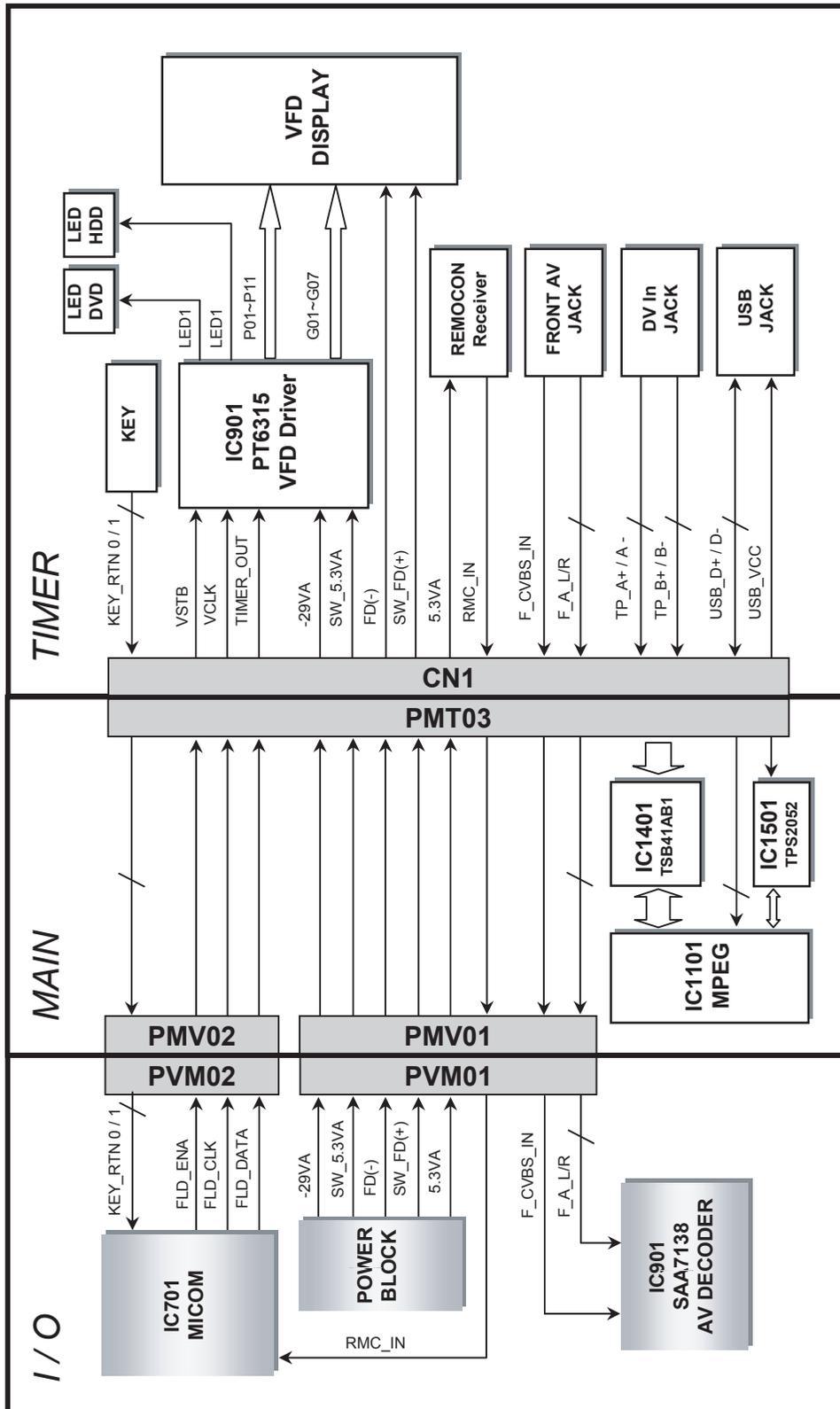
9. AUDIO OUTPUT BLOCK DIAGRAM



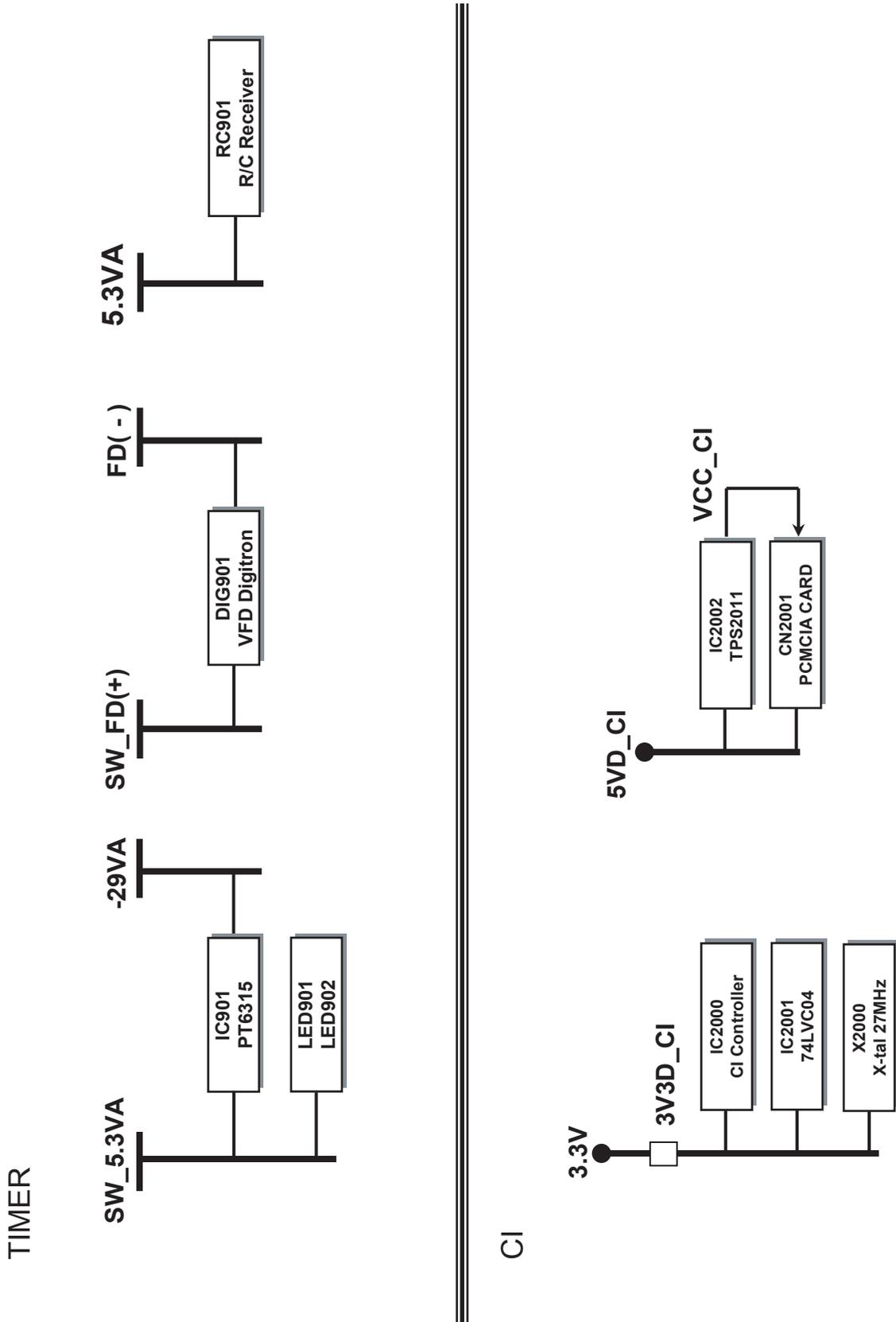
10. POWER I/O BLOCK DIAGRAM



11. FLD TIMER BOARD BLOCK DIAGRAM



12. POWER TIMER AND CI BLOCK DIAGRAM



CIRCUIT DIAGRAMS

1. SMPS CIRCUIT DIAGRAM

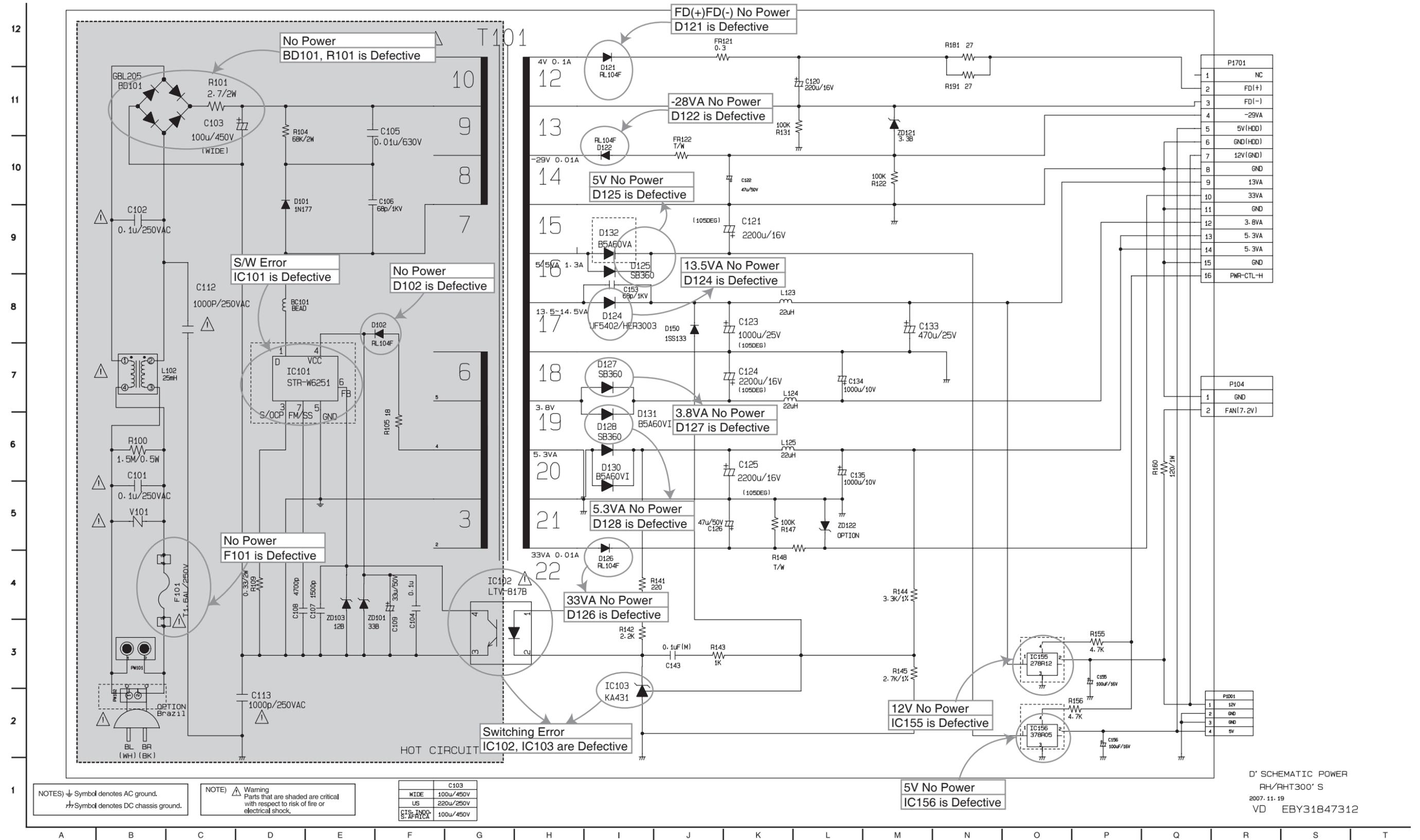
IMPORTANT SAFETY

WHEN SERVICING THIS CHASSIS, UNDER NO CIRCUMSTANCES SHOULD THE ORIGINAL DESIGN BE MODIFIED OR ALTERED WITHOUT PERMISSION FROM THE LG CORPORATION. ALL COMPONENTS SHOULD BE REPLACED ONLY WITH TYPES IDENTICAL TO THOSE IN THE ORIGINAL CIRCUIT. SPECIAL COMPONENTS ARE SHADED

ON THE SCHEMATIC FOR EASY IDENTIFICATION. THIS CIRCUIT DIAGRAM MAY OCCASIONALLY DIFFER FROM THE ACTUAL CIRCUIT USED. THIS WAY, IMPLEMENTATION OF THE LATEST SAFETY AND PERFORMANCE IMPROVEMENT CHANGES INTO THE SET IS NOT DELAYED UNTIL THE NEW SERVICE LITERATURE IS PRINTED.

NOTE :

1. Shaded parts are critical for safety. Replace only with specified part number.
2. Voltages are DC-measured with a digital voltmeter during Play mode.



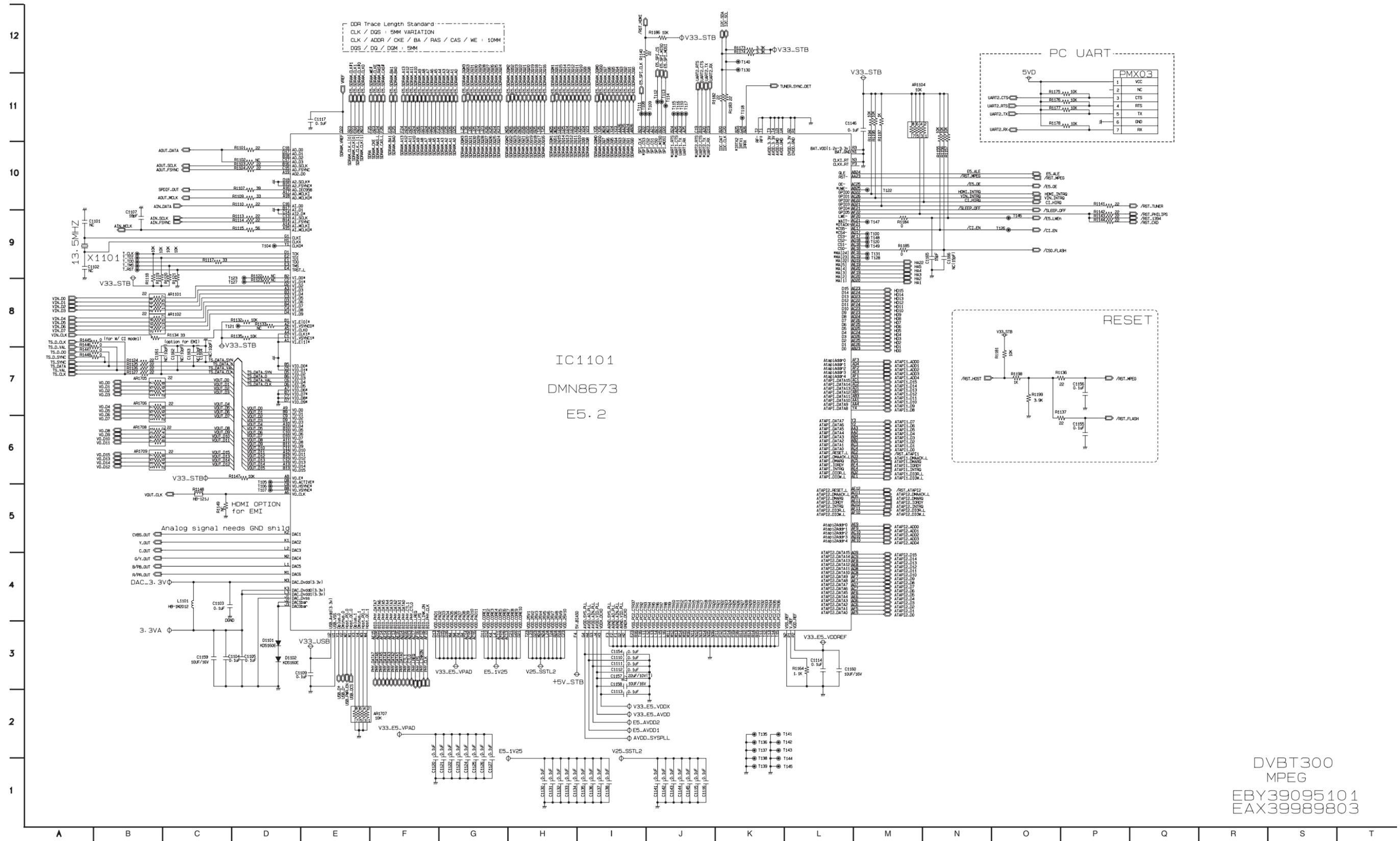
NOTES) ⚡ Symbol denotes AC ground.
 ⚡ Symbol denotes DC chassis ground.

NOTE) ⚡ Warning Parts that are shaded are critical with respect to risk of fire or electrical shock.

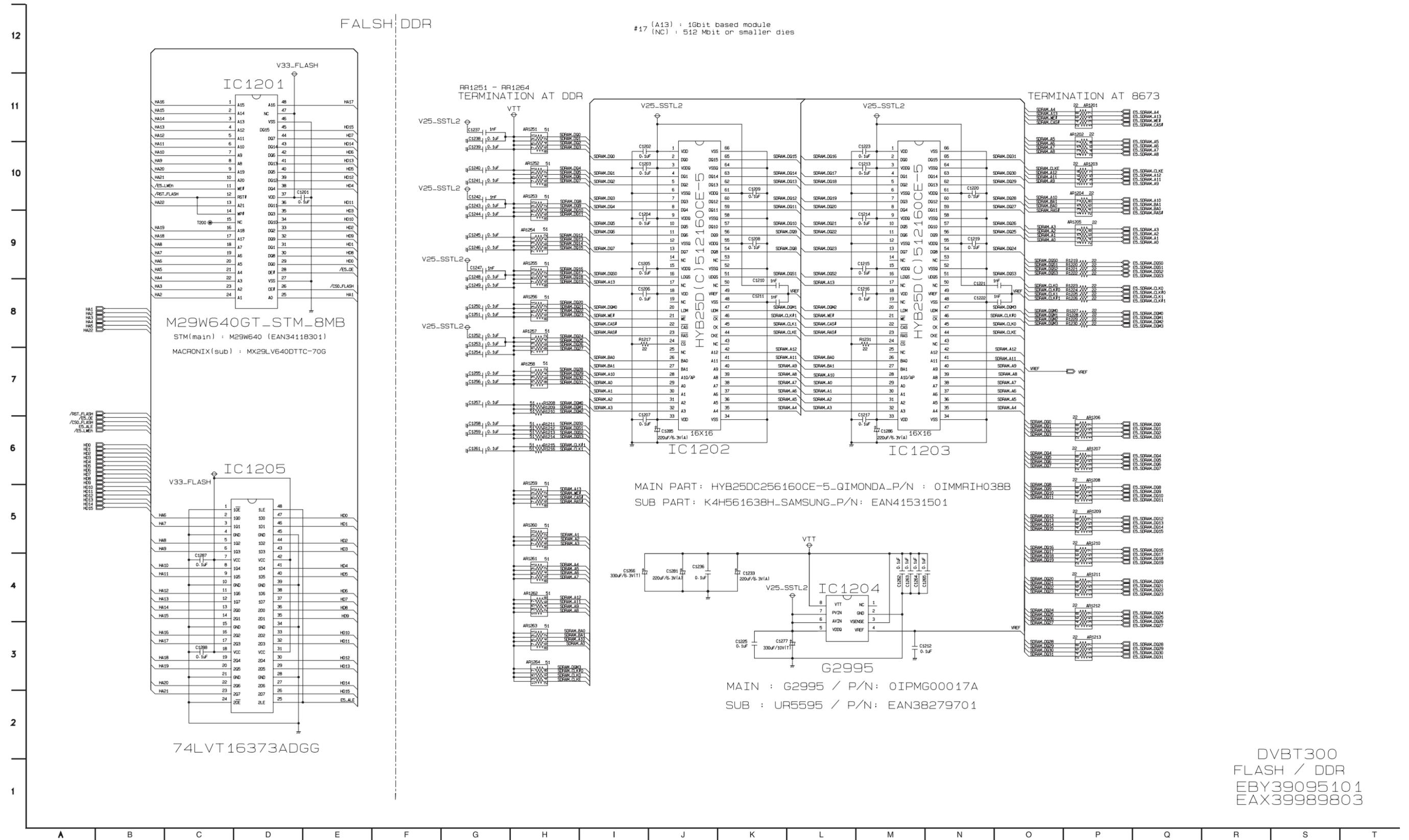
	C103
WIDE	100u/450V
US	220u/250V
CIS-TINDO-S-FRANCE	100u/450V

D' SCHEMATIC POWER
 RH/AHT300' S
 2007. 11. 19
 VD EBY31847312

2. MPEG CIRCUIT DIAGRAM

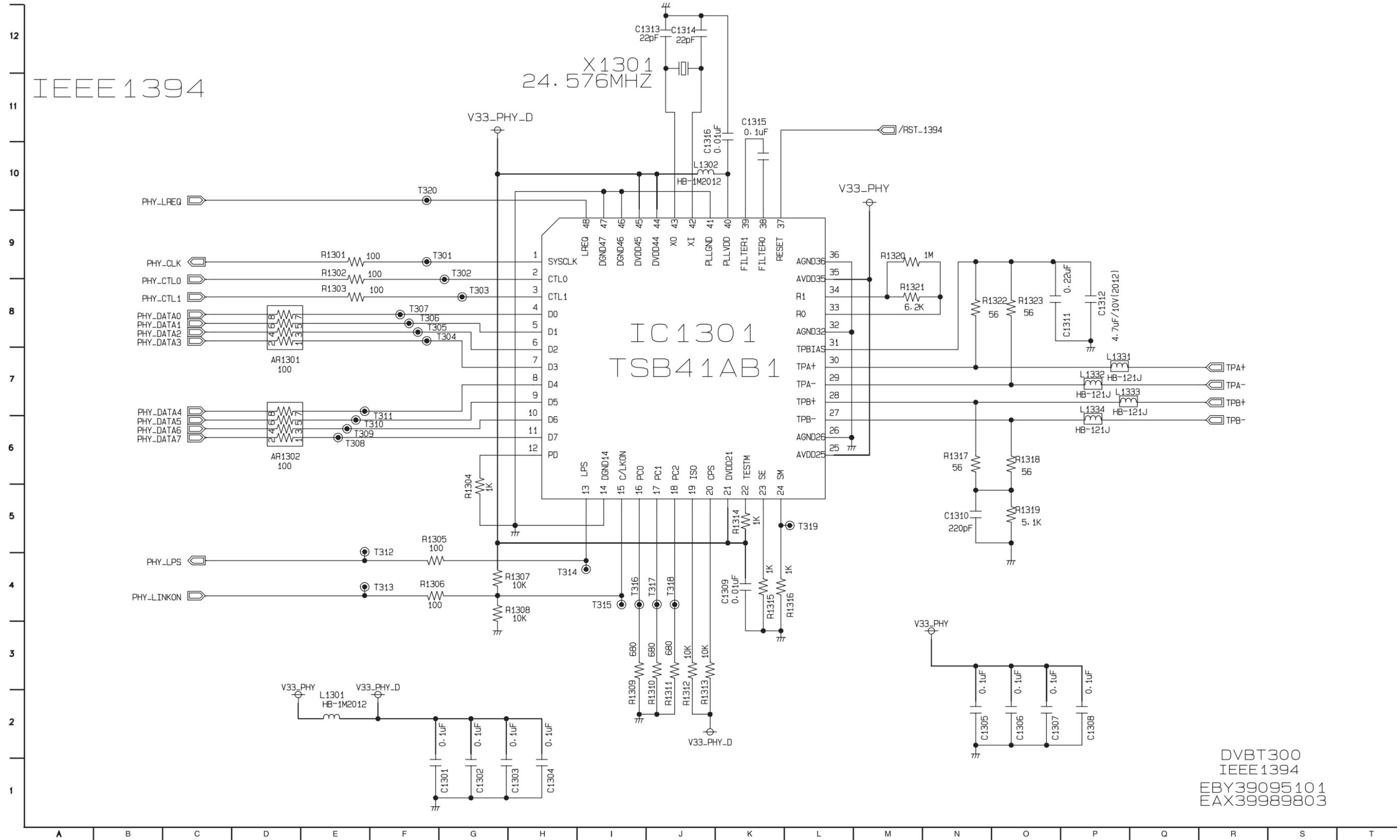


3. FLASH / DDR CIRCUIT DIAGRAM



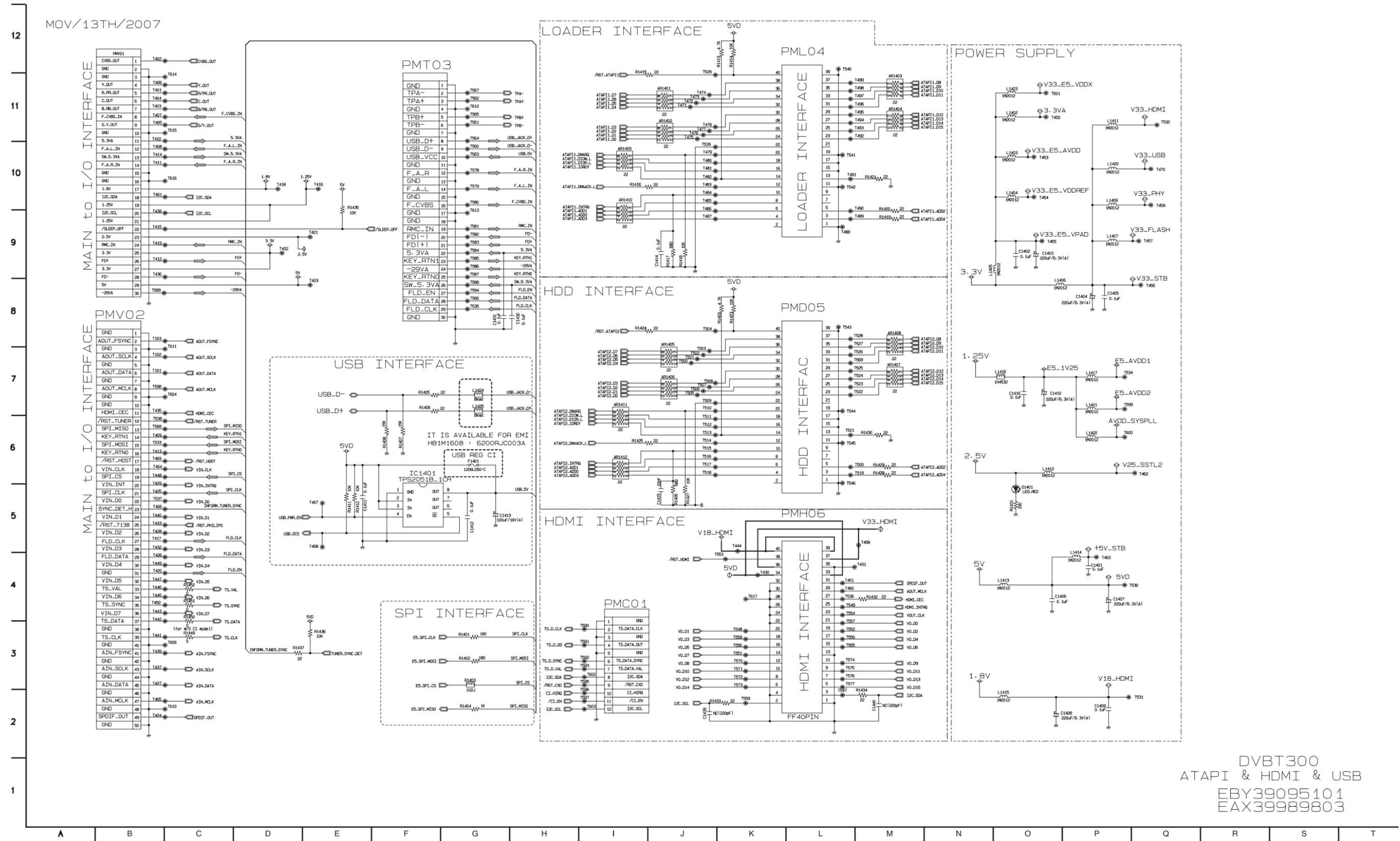
DVBT300
 FLASH / DDR
 EBY39095101
 EAX39989803

4. IEEE1394 CIRCUIT DIAGRAM



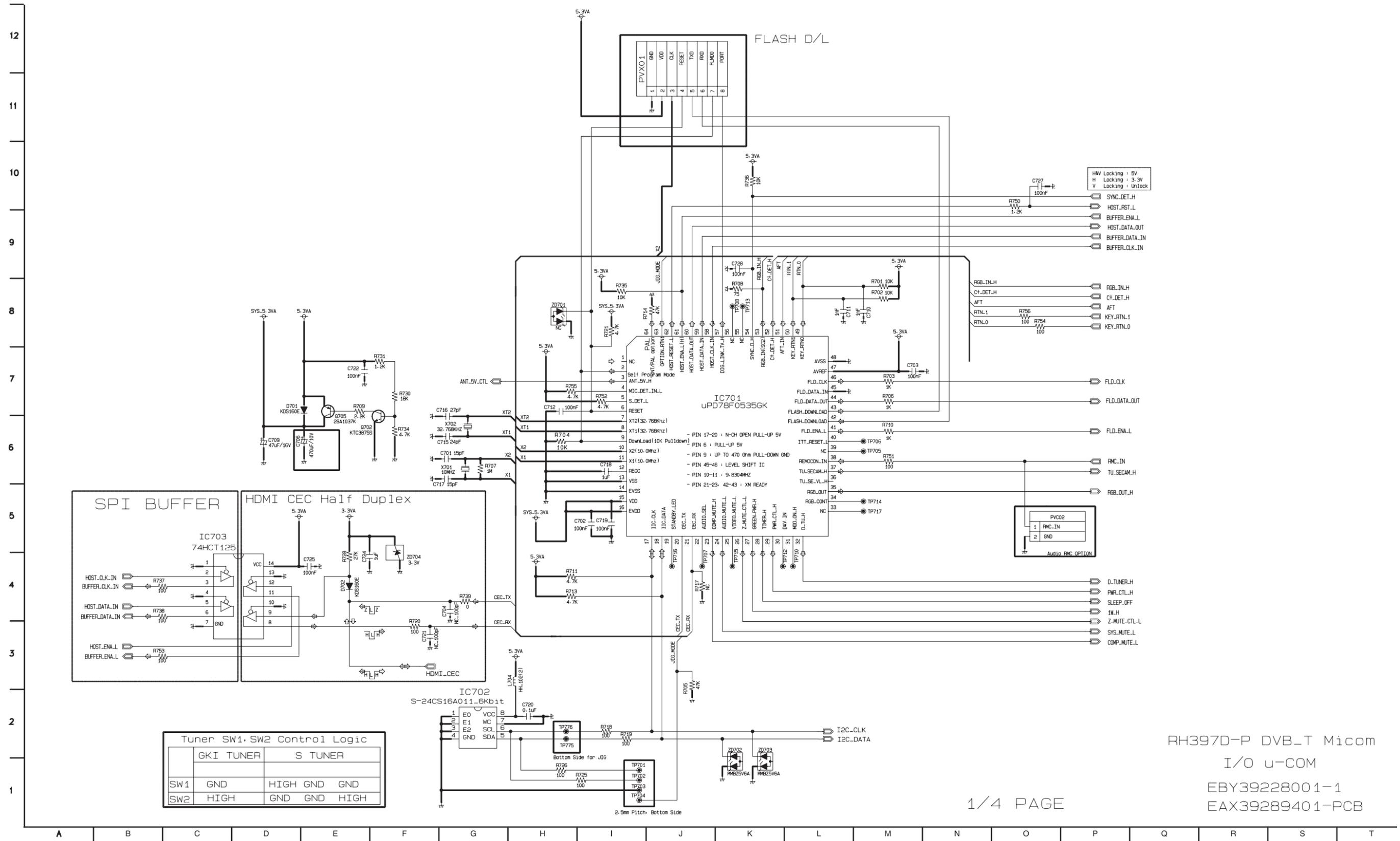
DVBT300
IEEE1394
EBY39095101
EAX39989803

5. ATAPI / HDMI / USB CIRCUIT DIAGRAM



DVBT300
ATAPI & HDMI & USB
EBY39095101
EAX39989803

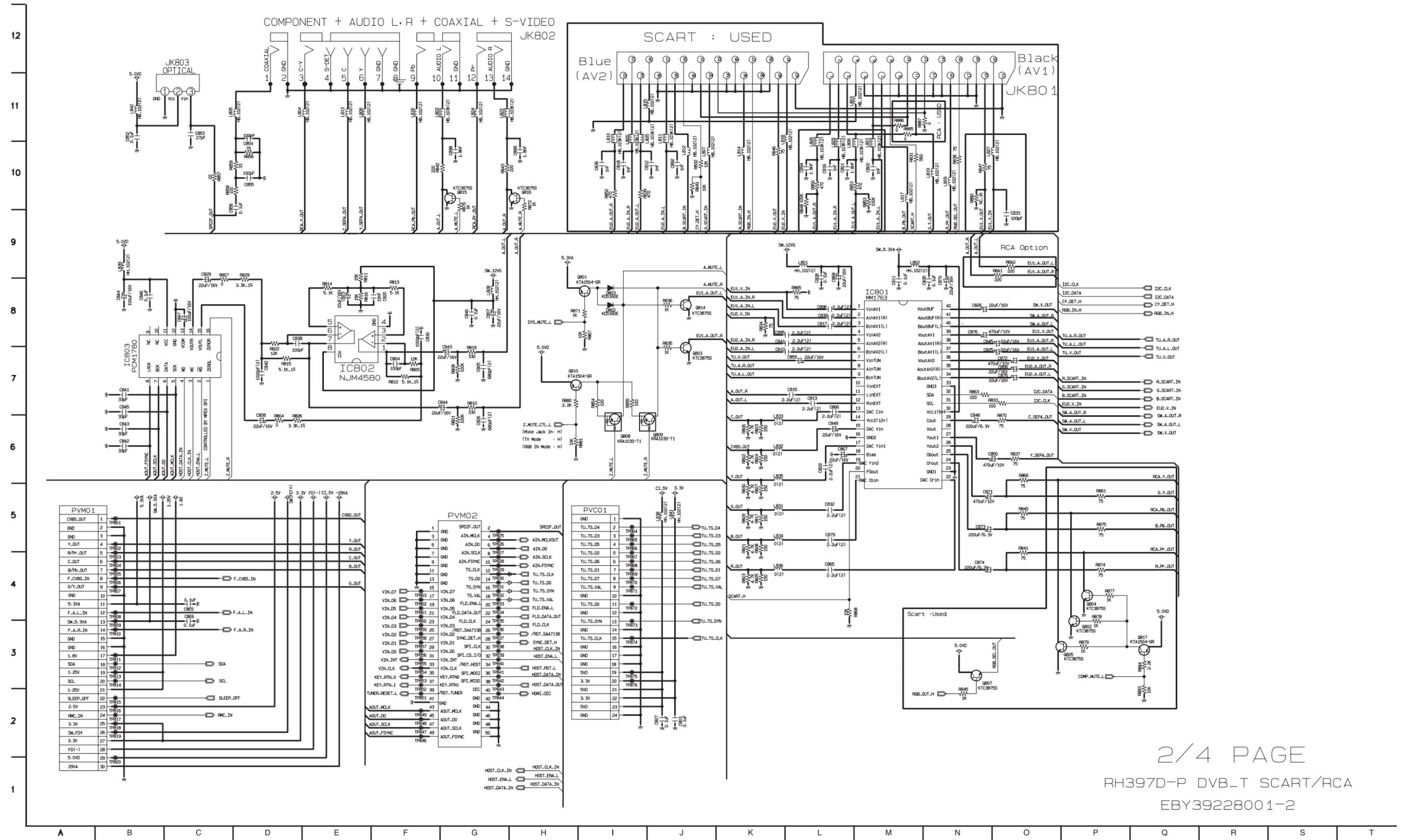
6. I/O μ-COM CIRCUIT DIAGRAM



1/4 PAGE

RH397D-P DVB-T Micom
I/O u-COM
EBY39228001-1
EAX39289401-PCB

7. SCART / RCA CIRCUIT DIAGRAM

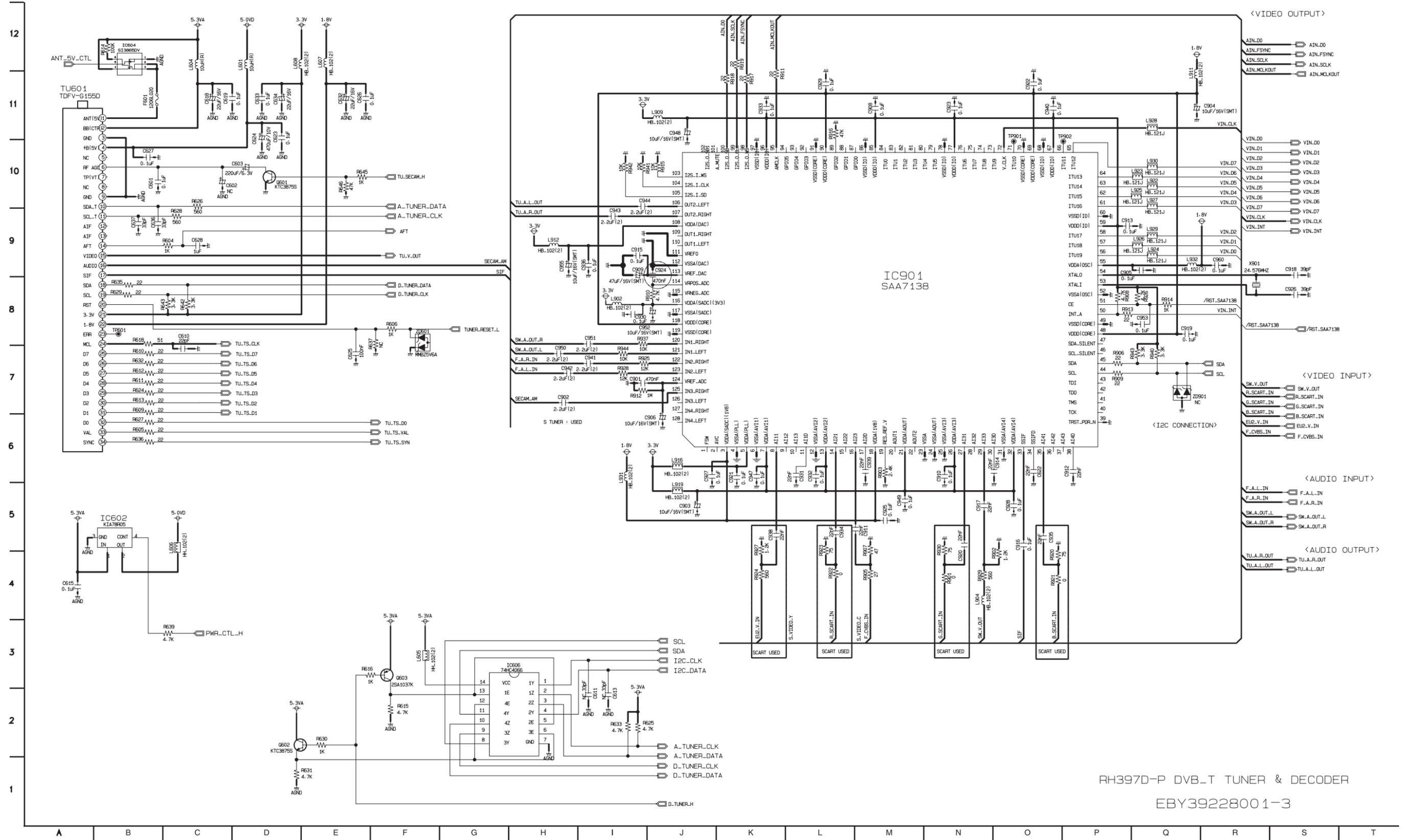


2/4 PAGE

RH397D-P DVB-T SCART/RCA

EBY39228001-2

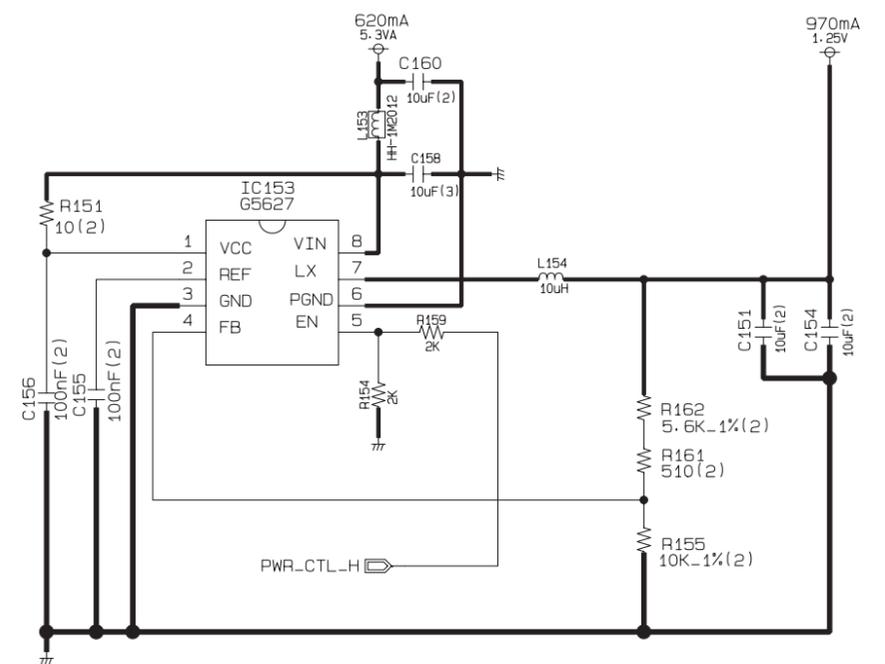
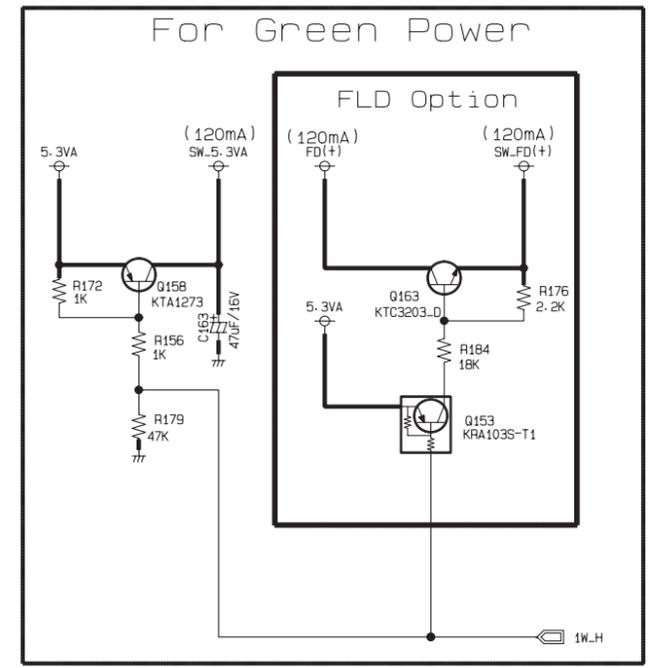
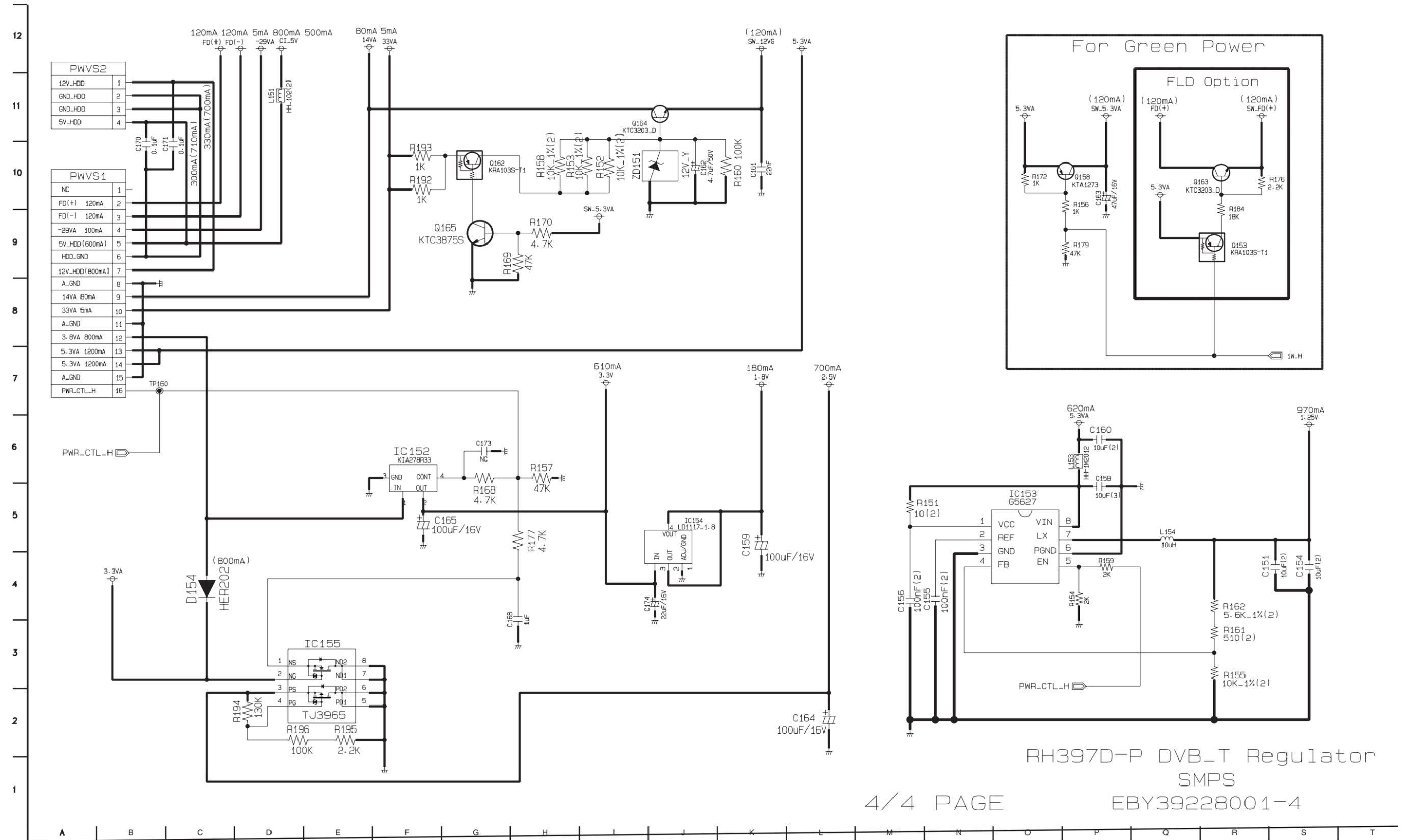
8. TUNER / DECODER CIRCUIT DIAGRAM



RH397D-P DVB-T TUNER & DECODER

EBY39228001-3

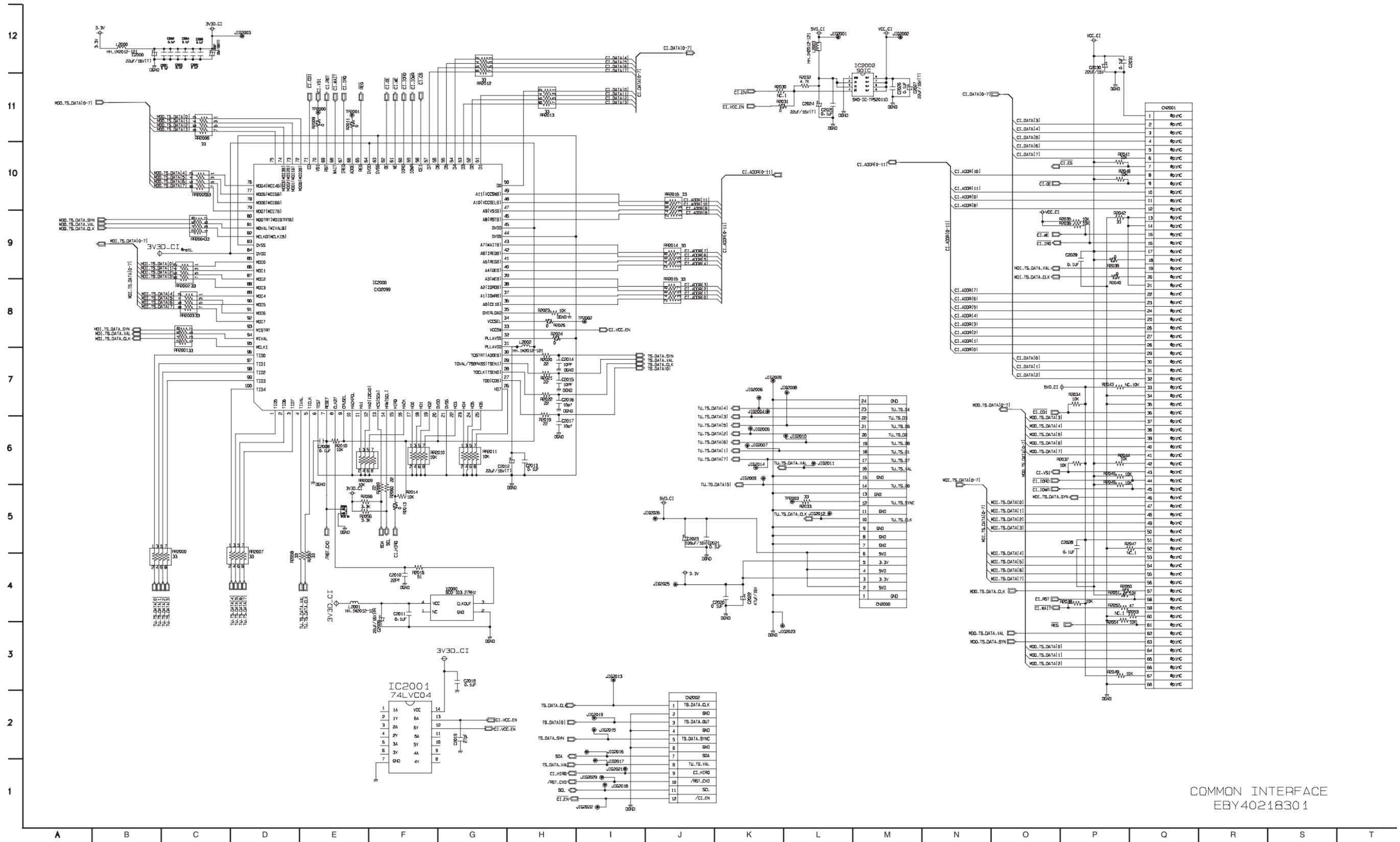
9. LDO CIRCUIT DIAGRAM



RH397D-P DVB-T Regulator
SMPS
EBY39228001-4

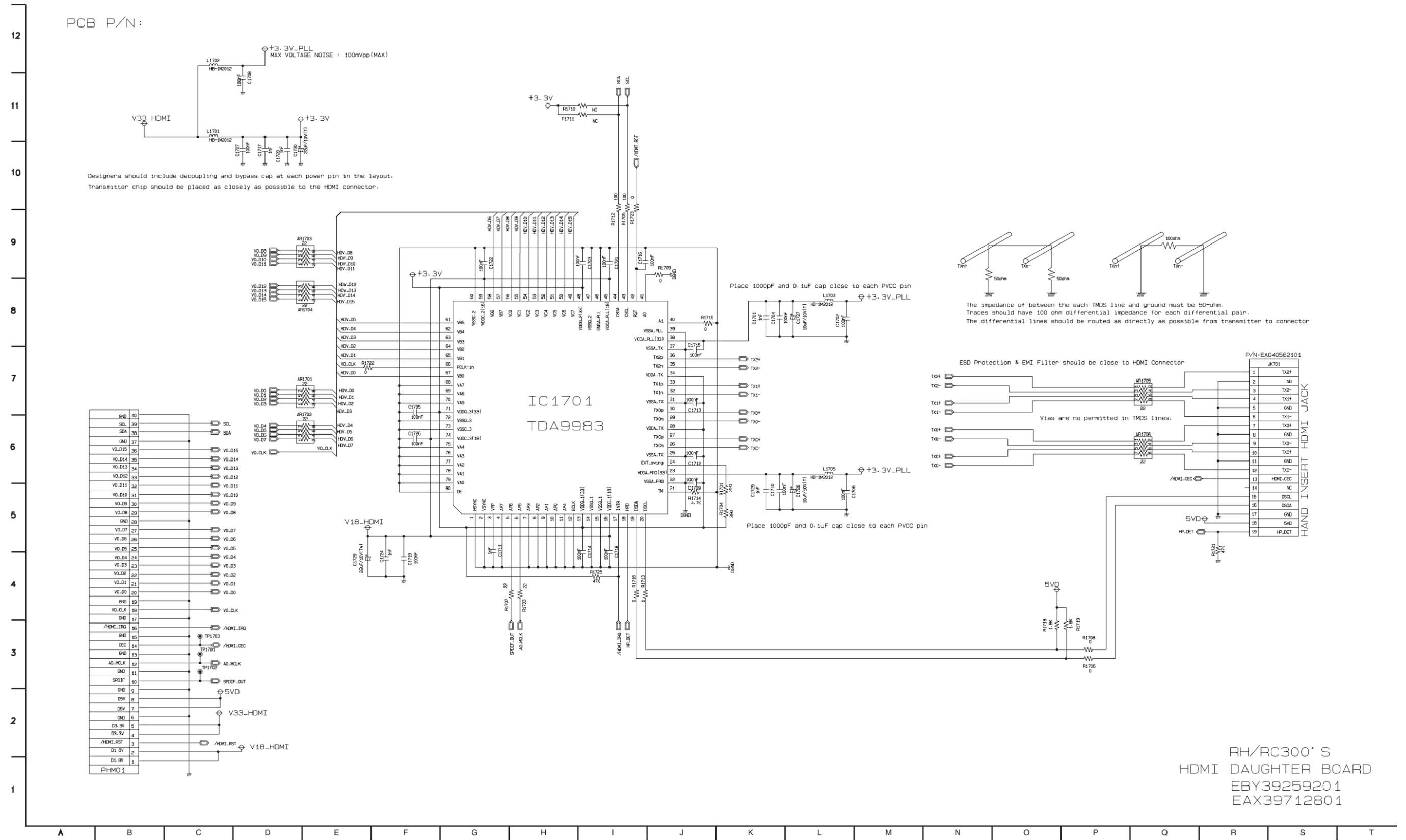
4/4 PAGE

10. COMMON INTERFACE BOARD CIRCUIT DIAGRAM(OPTIONAL)

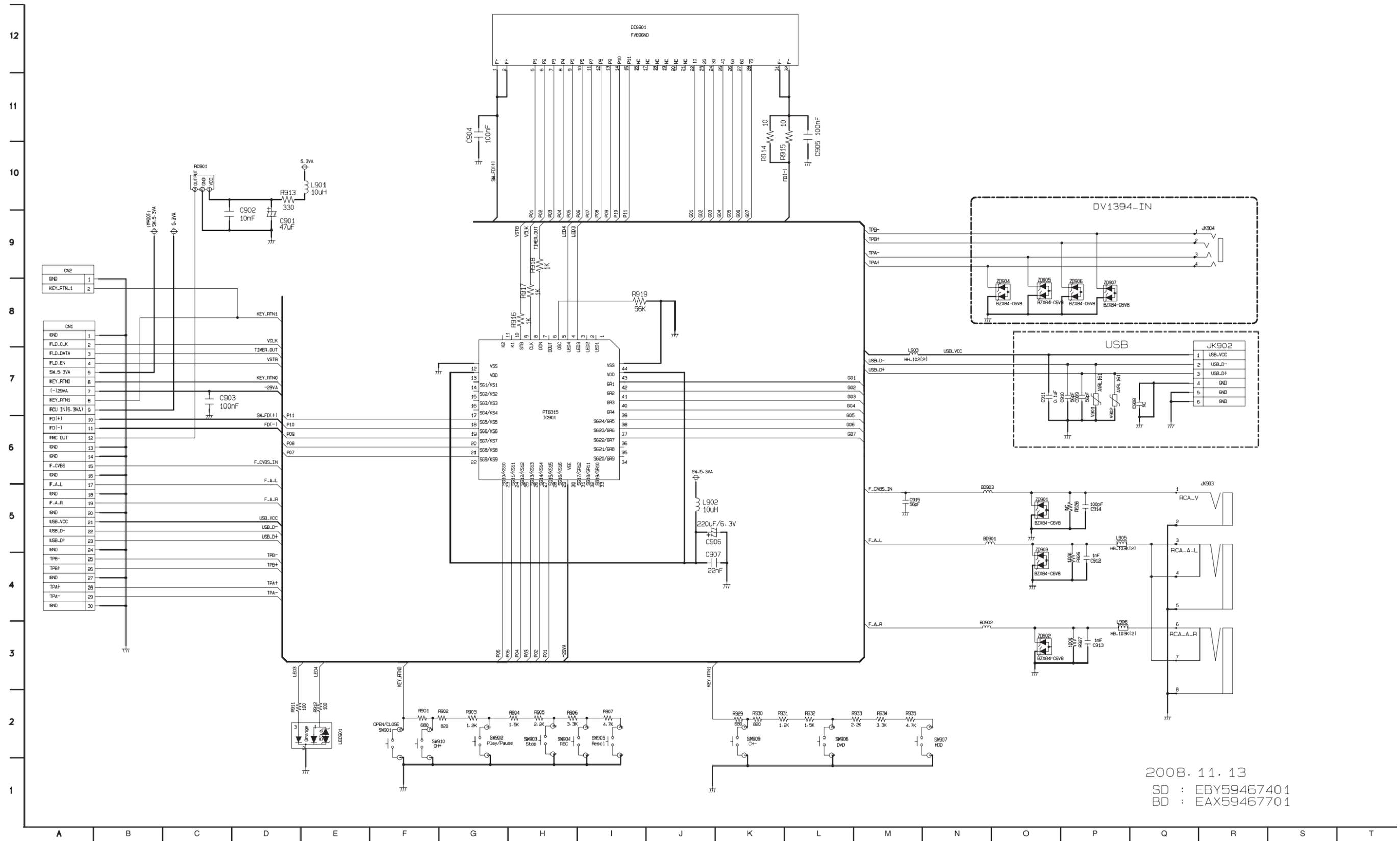


COMMON INTERFACE
EBY40218301

11. HDMI DAUGHTER BOARD CIRCUIT DIAGRAM

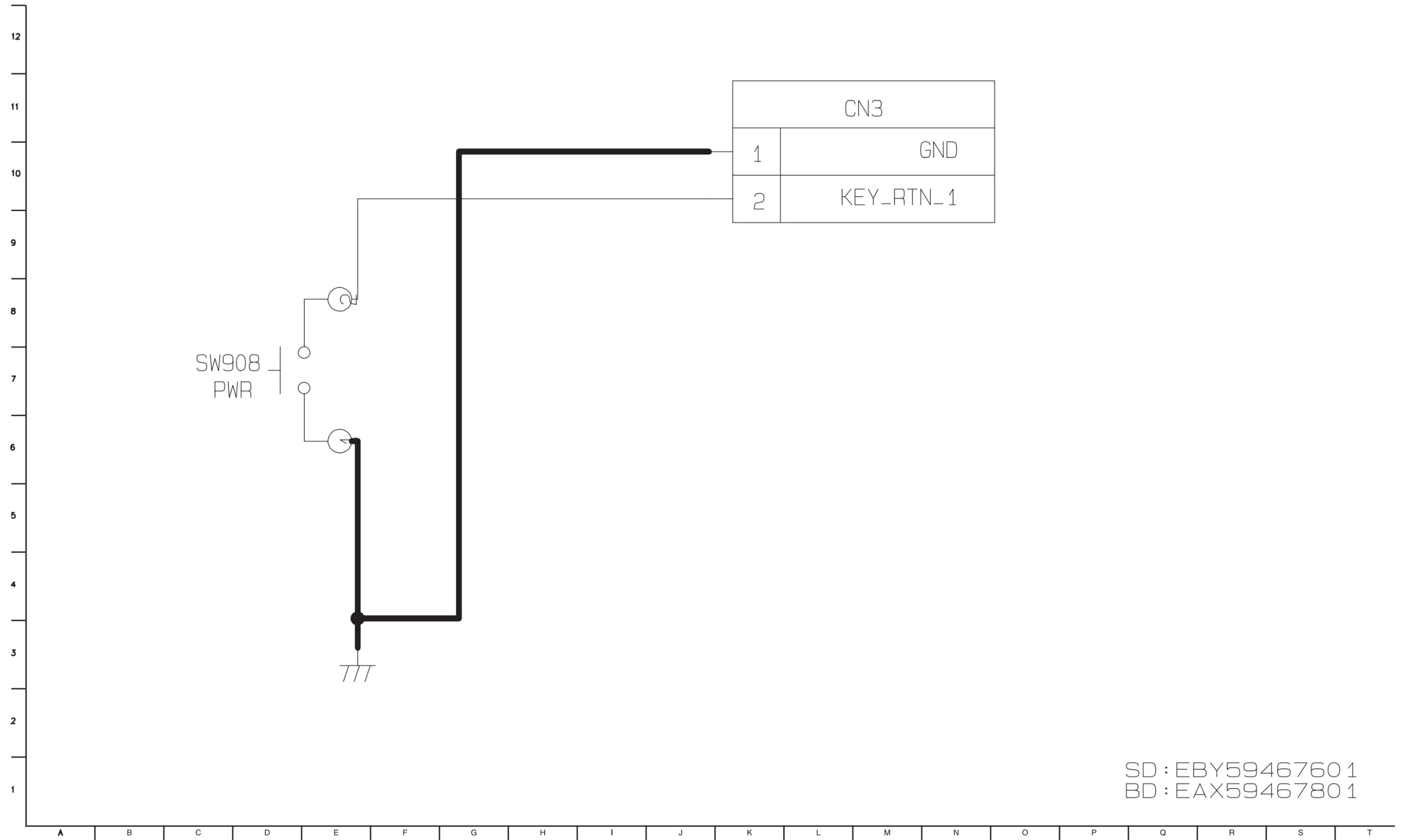


12. TIMER CIRCUIT DIAGRAM



2008. 11. 13
 SD : EBY59467401
 BD : EAX59467701

13. KEY CIRCUIT DIAGRAM



SD : EBY5946760 1
 BD : EAX5946780 1

CIRCUIT VOLTAGE CHART

1. ICs on MAIN BOARD (TOP)

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
IC1201 M29W640GT(STM_8MB) FLASH MEMORY IC201				
1	HA16	0.08	0.08	0.08
2	HA15	0.08	0.08	0.08
3	HA14	0.08	0.08	0.08
4	HA13	0.08	0.08	0.08
5	HA12	0.08	0.08	0.08
6	HA11	0.08	0.08	0.08
7	HA10	0.08	0.08	0.08
8	HA9	0.08	0.08	0.08
9	HA20	0.08	0.08	0.08
10	HA21	0.08	0.08	0.08
11	/E5_LWE _n	3.26	3.26	3.19
12	/RST_FLASH	4.00	4.00	4.00
13	HA22	0.00	0.00	0.10
14	/RST_FLASH(WP#)	4.00	4.00	4.00
15	NC	0.00	0.00	0.00
16	HA19	0.08	0.08	0.08
17	HA18	0.08	0.08	0.08
18	HA8	0.08	0.08	0.08
19	HA7	0.08	0.08	0.08
20	HA6	0.08	0.08	0.08
21	HA5	3.26	3.26	3.19
22	HA4	3.26	3.26	3.19
23	HA3	3.26	3.26	3.19
24	HA2	3.26	3.26	3.19
25	HA1	3.26	3.26	3.19
26	/CS0_FLASH	3.26	3.26	3.19
27	VSS	0.00	0.00	0.01
28	/E5_OE	3.26	3.26	3.19
29	HD0	0.00	0.00	0.01
30	HD8	0.00	0.00	0.01
31	HD1	0.00	0.00	0.01
32	HD9	0.00	0.00	0.01
33	HD2	0.00	0.00	0.01
34	HD10	0.00	0.00	0.01
35	HD3	0.00	0.00	0.01
36	HD11	0.00	0.00	0.01
37	VDD	3.28	3.28	3.25
38	HD4	0.00	0.00	0.01
39	HD12	0.00	0.00	0.01
40	HD5	0.00	0.00	0.01
41	HD13	0.00	0.00	0.01
42	HD6	0.00	0.00	0.01
43	HD14	0.00	0.00	0.01
44	HD7	0.00	0.00	0.01
45	HD15	0.00	0.00	0.01
46	VSS	0.00	0.00	0.01
47	V33_FLASH	3.28	3.28	3.25
48	HA17	0.08	0.08	0.08
IC1202 HYB25DC512160CE-5 16X16 DDR SDRAM IC1202				
1	VDD	2.42	2.42	2.41
2	SDRAM_DQ0	1.23	1.23	1.23
3	VDDQ	2.42	2.42	2.46
4	SDRAM_DQ1	1.10	1.10	1.10
5	SDRAM_DQ2	1.10	1.10	1.10
6	VSSQ	0.00	0.00	0.00
7	SDRAM_DQ3	1.10	1.10	1.07
8	SDRAM_DQ4	1.10	1.10	1.10
9	VDDQ	2.42	2.40	2.40
10	SDRAM_DQ5	1.10	1.07	1.07
11	SDRAM_DQ6	1.10	1.07	1.07
12	VSSQ	0.00	0.00	0.00

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
13	SDRAM_DQ7	1.10	1.03	1.03
14	NC	0.00	0.00	0.00
15	VDDQ	2.42	2.40	2.41
16	SDRAM_DQS0	1.20	1.19	1.19
17	SDRAM_A13	1.14	1.20	1.12
18	VDD	2.42	2.42	2.41
19	NC	0.00	0.00	0.00
20	SDRAM_DQM0	0.58	0.58	0.57
21	SDRAM_WE#	1.81	1.77	1.78
22	SDRAM_CAS#	1.76	1.67	1.70
23	SDRAM_RAS#	1.80	1.77	1.85
24	/CS	0.00	0.00	0.01
25	NC	0.00	0.00	0.00
26	SDRAM_BA0	1.21	1.21	1.22
27	SDRAM_BA1	1.20	1.20	1.22
28	SDRAM_A10	1.16	1.21	1.21
29	SDRAM_A0	1.15	1.10	1.21
30	SDRAM_A1	1.20	1.12	1.21
31	SDRAM_A2	1.16	1.12	1.13
32	SDRAM_A3	1.20	1.19	1.19
33	VDD	2.42	2.40	2.40
34	VSS	0.00	0.00	0.00
35	SDRAM_A4	1.20	1.19	1.19
36	SDRAM_A5	1.20	1.19	1.19
37	SDRAM_A6	1.20	1.19	1.19
38	SDRAM_A7	1.20	1.19	1.19
39	SDRAM_A8	1.20	1.19	1.19
40	SDRAM_A9	1.20	1.19	1.19
41	SDRAM_A11	1.16	1.11	1.13
42	SDRAM_A12	1.15	1.12	1.13
43	NC	0.00	0.00	0.00
44	SDRAM_CLKE	1.84	1.82	1.83
45	SDRAM_CLK1	1.23	1.22	1.22
46	SDRAM_CLK#1	1.18	1.18	1.18
47	SDRAM_DQM1	0.58	0.57	0.57
48	VSS	0.00	0.01	0.01
49	VREF	1.20	1.19	1.19
50	NC	0.00	0.00	0.00
51	SDRAM_DQS1	1.20	1.19	1.19
52	VSSQ	0.00	0.00	0.00
53	NC	0.00	0.00	0.00
54	SDRAM_DQ8	1.09	1.08	1.08
55	VDDQ	2.42	2.41	2.41
56	SDRAM_DQ9	1.10	1.09	1.09
57	SDRAM_DQ10	1.08	1.06	1.06
58	VSSQ	0.00	0.01	0.01
59	SDRAM_DQ11	1.08	1.03	1.03
60	SDRAM_DQ12	1.13	1.12	1.12
61	VDDQ	2.42	2.40	2.40
62	SDRAM_DQ13	1.08	1.05	1.05
63	SDRAM_DQ14	1.07	1.07	1.05
64	VSSQ	0.00	0.00	0.00
65	SDRAM_DQ15	1.10	1.08	1.03
66	VSS	0.00	0.00	0.00
IC1203 HYB25DC512160CE-5 16X16 DDR SDRAM IC1203				
1	VDD	2.42	2.42	2.41
2	SDRAM_DQ16	1.21	1.21	1.21
3	VDDQ	2.42	2.42	2.41
4	SDRAM_DQ17	1.21	1.21	1.20
5	SDRAM_DQ18	1.21	1.21	1.20
6	VSSQ	0.01	0.01	0.01
7	SDRAM_DQ19	1.21	1.21	1.20
8	SDRAM_DQ20	1.00	0.93	0.93

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
9	VDDQ	2.42	2.42	2.41
10	SDRAM_DQ21	1.21	1.21	1.20
11	SDRAM_DQ22	1.21	1.21	1.20
12	VSSQ	0.00	0.00	0.01
13	SDRAM_DQ23	1.21	1.21	1.20
14	NC	0.00	0.00	0.00
15	VDDQ	2.42	2.42	2.41
16	SDRAM_DQS2	0.85	0.85	0.89
17	SDRAM_A13	1.14	1.14	1.12
18	VDD	2.42	2.42	2.41
19	NC	0.00	0.00	0.00
20	SDRAM_DQM2	0.01	0.01	0.01
21	SDRAM_WE#	1.81	1.81	1.79
22	SDRAM_CAS#	1.76	1.76	1.71
23	SDRAM_RAS#	1.80	1.80	1.78
24	/CS	0.01	0.01	0.01
25	NC	0.00	0.00	0.00
26	SDRAM_BA0	1.22	1.22	1.21
27	SDRAM_BA1	1.21	1.21	1.21
28	SDRAM_A10	1.16	1.16	1.13
29	SDRAM_A0	1.16	1.16	1.13
30	SDRAM_A1	1.16	1.16	1.13
31	SDRAM_A2	1.16	1.16	1.14
32	SDRAM_A3	1.20	1.20	1.20
33	VDD	2.42	2.42	2.41
34	VSS	0.00	0.00	0.01
35	SDRAM_A4	1.20	1.20	1.20
36	SDRAM_A5	1.20	1.20	1.20
37	SDRAM_A6	1.20	1.20	1.20
38	SDRAM_A7	1.20	1.20	1.20
39	SDRAM_A8	1.20	1.20	1.20
40	SDRAM_A9	1.22	1.22	1.20
41	SDRAM_A11	1.14	1.12	1.14
42	SDRAM_A12	1.13	1.10	1.13
43	NC	0.00	0.00	0.00
44	SDRAM_CLKE	1.86	1.86	1.84
45	SDRAM_CLK0	1.24	1.24	1.23
46	SDRAM_CLK#0	1.21	1.21	1.19
47	SDRAM_DQM3	0.56	0.56	0.55
48	VSS	0.01	0.01	0.01
49	VREF	1.21	1.21	1.19
50	NC	0.00	0.00	0.00
51	SDRAM_DQS1	0.82	0.82	0.89
52	VSSQ	0.00	0.00	0.00
53	NC	0.00	0.00	0.00
54	SDRAM_DQ24	1.22	1.22	1.20
55	VDDQ	2.45	2.45	2.41
56	SDRAM_DQ25	1.22	1.22	1.19
57	SDRAM_DQ26	1.22	1.22	1.01
58	VSSQ	0.00	0.00	0.01
59	SDRAM_DQ27	1.22	1.22	1.38
60	SDRAM_DQ28	1.22	1.22	1.35
61	VDDQ	2.45	2.45	2.41
62	SDRAM_DQ29	1.22	1.22	1.20
63	SDRAM_DQ30	1.16	1.16	1.22
64	VSSQ	0.01	0.01	0.01
65	SDRAM_DQ31	1.22	1.22	1.35
66	VSS	0.00	0.00	0.01
IC1204 G2995 IC204				
1	NC	0.00	0.00	0.00
2	GND	0.00	0.00	0.00
3	VSENSE	1.21	1.21	1.21
4	VREF	1.20	1.19	1.19

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
5	VDDQ	2.42	2.40	2.41
6	AVIN	2.42	2.40	2.41
7	PVIN	2.42	2.40	2.41
8	VTT	1.21	1.21	1.21
IC1301 TSB41AB1 IEEE1394-DV Input IC401				
1	PHY_CLK	1.67	1.67	1.69
2	PHY_CTL0	0.01	0.01	0.01
3	PHY_CTL1	0.01	0.01	0.01
4	PHY_DATA0	0.01	0.01	0.01
5	PHY_DATA1	0.01	0.01	0.01
6	PHY_DATA2	0.01	0.01	0.01
7	PHY_DATA3	0.01	0.01	0.01
8	PHY_DATA4	0.01	0.01	0.01
9	PHY_DATA5	0.01	0.01	0.01
10	PHY_DATA6	0.01	0.01	0.01
11	PHY_DATA7	0.01	0.01	0.01
12	1394_PD	0.01	0.01	0.01
13	PHY_LPS	3.19	3.19	3.20
14	GND	0.00	0.00	0.00
15	PHY_LINKON	0.02	0.02	0.02
16	PC0	0.01	0.01	0.01
17	PC1	0.01	0.01	0.01
18	PC2	0.01	0.01	0.01
19	ISO	3.24	3.24	3.24
20	CPS	3.24	3.24	3.24
21	DVDD21	3.24	3.24	3.24
22	TESTM	3.24	3.24	3.24
23	SE	0.01	0.01	0.01
24	SM	0.01	0.01	0.01
25	AVDD25	3.24	3.24	3.24
26	GND	0.00	0.00	0.00
27	TPB-	1.57	1.57	1.57
28	TPB+	1.78	1.78	1.78
29	TPA-	1.85	1.85	1.85
30	TPA+	1.78	1.78	1.78
31	TPBIAS	1.83	1.83	1.83
32	AGND32	0.01	0.01	0.01
33	RO	0.01	0.01	0.01
34	RI	1.21	1.21	1.21
35	AVDD35	3.24	3.24	3.24
36	GND	0.00	0.00	0.00
37	/RST_PHY	3.21	3.20	3.20
38	FILTER0	0.01	0.01	0.01
39	FILTER1	1.27	1.28	1.28
40	PLLVD	3.26	3.24	3.24
41	PLLGND	0.00	0.00	0.00
42	XI	1.49	1.48	1.48
43	XO	1.49	1.49	1.49
44	DVDD44	3.26	3.24	3.24
45	DVDD45	3.26	3.24	3.24
46	GND	0.00	0.00	0.00
47	GND	0.00	0.00	0.00
48	PHY_LREQ	0.01	0.01	0.01
IC1401 TPS2051B_1CH USB INTERFACE IC1401				
1	GND	0.00	0.00	0.00
2	IN	4.96	4.96	4.96
3	IN	4.96	4.96	4.96
4	USB_PWR_EN	0.05	0.05	0.05
5	USB_OCS	4.95	4.95	4.94
6	OUT	4.95	4.94	4.94
7	OUT	4.93	4.94	4.94
8	USB_5V	4.92	4.90	4.92

2. ICs on MAIN BOARD (BOTTOM)

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
IC1205 74LV16373 ADDRESS LATCH IC1205 </				

- INFORMATION :**
 1. Voltage Check using RH300 DV1
 2. EE Mode : Check with Signal C2
 3. Playback Mode : Check with DVD TEST DISC KDV-N Chapter 2
 4. Record Mode : Check with recording signal C2 using DVD -RW
 Brand : Mitsubishi, VR Mode

3. ICs on I/O BOARD

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
IC151 KIA78R25				
1	IN	3V	3V	3V
2	OUT	2.48V	2.48V	2.48V
3	GND	0V	0V	0V
4	CONTROL	3.9V	3.9V	3.9V
IC152 KIA278R33				
1	IN	3.68V	3.68V	3.68V
2	OUT	3.28V	3.28V	3.28V
3	GND	0V	0V	0V
4	CONTROL	4.47V	4.47V	4.47V
IC153 G5627				
1	VCC	5.23V	5.23V	5.23V
2	REF	0.79V	0.79V	0.79V
3	GND	0V	0V	0V
4	FB	0.8V	0.8V	0.8V
5	EN	2.6V	2.6V	2.6V
6	PGND	0.05V	0.05V	0.05V
7	LX	1.37V	1.37V	1.37V
8	VIN	5.23V	5.23V	5.23V
IC154 LD1117 1.8				
1	ADJ/GND	0V	0V	0V
2	OUT	1.8V	1.8V	1.8V
3	IN	3.19V	3.19V	3.17V
4	VOUT	1.8V	1.8V	1.8V
IC602 KIA78R05				
1	IN	5.2V	5.2V	5.2V
2	OUT	4.97V	4.97V	4.97V
3	GND	0V	0V	0V
4	CONTROL	3.76V	3.76V	3.76V
IC604 SI3865DV				
1	GND	0V	0V	0V
2	ANT(5V)	0.02V	0.03V	0.03V
3	ANT(5V)	0.02V	0.03V	0.03V
4	VCC (5.3V)	5.2V	5.2V	5.2V
5	ANT_5V_CTL	0V	0V	0V
6	VCC (100K/5.3V)	5.15V	5.15V	5.15V
IC606 74HC4066				
1	I2C_CLK	4.93V	4.93V	4.93V
2	A_TUNER_CLK	4.93V	4.93V	4.93V
3	A_TUNER_DATA	4.93V	4.93V	4.93V
4	I2C_DATA	4.93V	4.93V	4.93V
5	2E	5.2V	5.2V	5.2V
6	PWR_CTL_H	0V	0V	0V
7	GND	0V	0V	0V
8	SCL	2.41V	2.46V	2.7V
9	D_TUNER_CLK	2V	2.7V	2V
10	D_TUNER_DATA	2V	2.7V	2V
11	SDA	2.37V	2.4V	2.7V
12	PWR_CTL_H	0V	0V	0V
13	1E	5.2V	5.2V	5.2V
14	VCC	5.21V	5.21V	5.21V
IC701 UPD78F0535GK				
1	NC	5.19V	5.2V	5.19V
2	FLMD0	0V	0.01V	0V
3	ANT_5V_CTL	0V	0.01V	0V
4	MIC_DET_IN_L	0.55V	0.66V	0.55V
5	S_DET_L	0V	0.01V	0V
6	RESET	5.2V	5.2V	5.2V
7	XT2 (32.7 KHZ)	2.95V	3.07V	3.02V
8	XT1 (32.7 KHZ)	2.08V	3.2V	2.12V
9	FLMD0	0V	0V	0V

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
10	X2 (10 MHz)	3.1V	3.22V	3.18V
11	X1 (10 MHz)	2.58V	2.61V	2.61V
12	REGC	2.52V	2.52V	2.52V
13	VSS	0V	0V	0V
14	EVSS	0V	0V	0V
15	VDD	5.2V	5.2V	5.2V
16	EVDD	5.2V	5.2V	5.2V
17	I2C_CLK	4.95V	4.94V	4.95V
18	I2C_DATA	4.95V	4.94V	4.95V
19	STANBY_LED	0.6V	0.61V	0.62V
20	CEC_TX	3.04V	2.98V	3V
21	CEC_RX	5.24V	5.24V	5.23V
22	AUDIO_SEL	0.01V	0.01V	0.01V
23	COMP_MUTE_H	5.2V	5.2V	5.19V
24	AUDIO_MUTE_L	5.18V	5.17V	5.17V
25	VIDEO_MUTE_L	5.2V	5.19V	5.19V
26	Z_MUTE_CTL_L	5.17V	5.17V	5.17V
27	GREEN_PWR_H	0.09V	0.1V	0.09V
28	TIMER_H	5.19V	5.19V	5.19V
29	POWER_CTL_H	5.17V	5.12V	5.12V
30	DAV_IN	0.6V	0.46V	0.51V
31	MOD_ON_H	0.02V	0.02V	0.02V
32	D_TU_H	0.09V	0.09V	0.09V
33	SYNC_D_H	5.03V	5.03V	5.03V
34	RGB_CONT	0.02V	0.02V	0.02V
35	RGB_OUT	0.02V	0.02V	0.02V
36	TU_SE_VL_H	0.02V	0.02V	0.02V
37	TU_SECAM_H	0.02V	0.02V	0.02V
38	REMOCON_IN	4.88V	4.88V	4.88V
39	NC	0.02V	0.02V	0.02V
40	ITT_RESET_L	0.02V	0.02V	0.02V
41	FLD_ENA_L	4.91V	4.97V	4.97V
42	TXD	5.19V	5.19V	5.19V
43	RXD	0.02V	0.02V	0.02V
44	FLD_DATA_OUT	0.75V	0.75V	0.74V
45	FLD_DATA_IN	0V	0V	0V
46	FLD_CLK	5.14V	5.14V	5.13V
47	AVREF	5.24V	5.24V	5.24V
48	AVSS	0V	0V	0V
49	KEY_RTN_0	5.24V	5.24V	5.23V
50	KEY_RTN_1	5.24V	5.24V	5.23V
51	AFT_IN	3.1V	3.1V	3.1V
52	C+_DET_H	0V	0.01V	0.01V
53	RGB_IN_H	0.09V	0.09V	0.09V
54	NC	5.03V	5.03V	5.03V
55	NC	0V	0.01V	0V
56	NC	4.42V	4.42V	4.42V
57	DIG_LINK_TV_H	5.2V	5.19V	5.19V
58	HOST_CLK_IN	5.03V	5.03V	5.03V
59	HOST_DATA_IN	0V	0.01V	0V
60	HOST_DATA_OUT	0.43V	0.43V	0.43V
61	HOST_ENA_L	5.19V	5.19V	5.19V
62	HOST_RESET_L	5.14V	5.14V	5.14V
63	OPTION_RTN1	0.52V	0.42V	0.55V
64	NT/PAL OPTION	0V	0V	0V
IC702 S-24CS16A011 6Kbit				
1	E0	0V	0V	0V
2	E1	0V	0V	0V
3	E2	0V	0V	0V
4	GND	0V	0V	0V
5	I2C_DATA	4.95V	4.95V	4.95V
6	I2C_CLK	4.94V	4.94V	4.94V
7	WC	0V	0V	0V

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
8	VCC	5.24V	5.24V	5.24V
IC703 74HCT125				
1	GND	0V	0V	0V
2	HOST_CLK_IN	3.05V	3.05V	3.04V
3	BUFFER_DATA_IN	5.03V	5.03V	5.02V
4	GND	0V	0V	0V
5	HOST_DATA_IN	0.02V	0.02V	0.02V
6	BUFFER_CLK_IN	0.01V	0.01V	0.01V
7	GND	0V	0V	0V
8	CEC_RX	5.24V	5.24V	5.24V
9	CEC_TX	3.04V	2.99V	3.04V
10	GND	0V	0V	0V
11	BUFFER_ENA_L	5.24V	5.24V	5.24V
12	HOST_ENA_L	3.18V	3.18V	3.18V
13	GND	0V	0V	0V
14	VCC (5.3VA)	5.24V	5.24V	5.24V
IC801 MM1763				
1	EU1_V_IN	1.07V	1.07V	1.07V
2	EU1_A_IN_R	7.05V	7.05V	0.01V
3	EU1_A_IN_L	7.05V	7.05V	0.01V
4	EU2_V_IN	1.07V	1.07V	1.07V
5	EU2_A_IN_R	7.06V	7.06V	7.06V
6	EU2_A_IN_L	7.06V	7.06V	7.06V
7	TU_V_OUT	1.6V	1.69V	1.6V
8	TU_A_R_OUT	7.08V	7.08V	7.08V
9	TU_A_L_OUT	7.08V	7.08V	7.08V
10	VinEXT (NC)	1.07V	1.07V	1.07V
11	A_OUT_R	7.06V	7.06V	7.06V
12	A_OUT_L	7.06V	7.06V	7.06V
13	C_OUT	2.45V	2.45V	2.45V
14	VCC2 (12 V)	12.15V	12.15V	12.15V
15	CVBS_OUT	1.51V	1.5V	1.51V
16	GND2	0V	0V	0V
17	Y_OUT	1.06V	1.06V	1.06V
18	BIAS	2.46V	2.46V	2.46V
19	G_OUT	1.07V	1.07V	1.07V
20	Fsout	9.89V	9.89V	9.89V
21	B_OUT	2.45V	2.45V	2.45V
22	R_OUT	2.45V	2.45V	2.45V
23	GND1	0V	0V	0V
24	R_Pr_OUT	2.52V	2.52V	2.52V
25	B_Pb_OUT	2.52V	2.52V	2.52V
26	G_Y_OUT	1.11V	1.11V	1.11V
27	Y_SEPA_OUT	1.09V	1.09V	1.09V
28	VOUT (NC)	2V	2V	2V
29	C_SEPA_OUT	2.52V	2.52V	2.52V
30	VCC1 (5V)	5.16V	5.16V	5.16V
31	I2C_CLK	4.93V	4.93V	4.93V
32	I2C_DATA	4.93V	4.93V	4.93V
33	GND3	0V	0V	0V
34	EU2_A_OUT_L	6.48V	6.48V	6.48V
35	EU2_A_OUT_R	6.48V	6.48V	6.48V
36	EU2_V_OUT	2.02V	2.02V	2.02V
37	EU1_A_OUT_L	6.48V	6.48V	6.48V
38	EU1_A_OUT_R	6.48V	6.48V	6.48V
39	EU1_V_OUT	2.02V	2.02V	2.02V
40	SW_A_OUT_R	6.48V	6.48V	6.47V
41	SW_A_OUT_L	6.48V	6.48V	6.47V
42	SW_V_OUT	1.6V	1.6V	1.61V
IC802 NJM4580				
1	A_OUT_L	6.1V	6.1V	6.09V
2	DAC_A_L	6.1V	6.1V	6.09V

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
3	VCC1	6.1V	6.1V	6.09V
4	GND	0V	0V	0V
5	VCC2	6.1V	6.1V	6.09V
6	DAC_A_R	6.1V	6.1V	6.09V
7	A_OUT_R	6.1V	6.1V	6.09V
8	VCC (12V)	12.2V	12.2V	12.19V
IC803 PCM1780 AUDIO DAC				
1	Z_MUTE_L	4.95	4.95	4.95
2	E5_SPI_CS	3.26	3.26	3.18
3	E5_SPI_CLK	3.13	3.12	3.07
4	E5_SPI_MOSI	0.02	0.02	0.02
5	AOUT_MCLK	1.65	1.66	1.62
6	AOUT_DATA	1.63	1.60	1.60
7	AOUT_SCLK	1.64	1.63	1.61
8	AOUT_FSYNC	1.63	1.63	1.60
9	NC	0.00	0.00	0.00
10	NC	0.00	0.00	0.00
11	VCC	4.95	4.95	4.95
12	GND	0.00	0.00	0.00
13	VCOM	2.47	2.49	2.49
14	AOUT_R	2.42	2.42	2.42
15	AOUT_L	2.42	2.42	2.42
16	Z_MUTE_R	4.95	4.95	4.95
IC901 SAA7138				
1	FSW (NC)	0.47V	0.48V	0.62V
2	AVC (NC)	0.47V	0.62V	0.62V
3	VDDA (SADC) (1.8V)	1.78V	1.78V	1.78V
4	VSSA (PLL)	0.02V	0.02V	0.02V
5	VDDA (PLL)	3.18V	3.18V	3.18V
6	VSSA (AV11)	0V	0V	0V
7	VDDA (AV11)	3.17V	3.17V	3.17V
8	EU2_V_IN (AI11)	0.58V	0.58V	0.58V
9	AI12	0.58V	0.58V	0.58V
10	AI13	0.58V	0.58V	0.58V
11	AI10	1V	1V	1V
12	VSSA(AVI2)	0V	0V	0V
13	VDDA (AVI2)	3.17V	3.17V	3.16V
14	R_SCART_IN (AI21)	0.56V	0.56V	0.56V

4. DMN8673

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
IC1101 LSI DMN8673				
IC101				
A1	VI_E[1]	1.17	1.19	1.17
A2	VI_VSYNC[0]	0.00	0.00	0.00
A3	VI_D[3]	1.37	1.36	1.36
A4	VI_CLK[1]	0.00	0.00	0.00
A5	VI_CLK[0]	1.61	1.64	1.64
A6	VO_CLK	1.60	1.62	1.62
A7	VIO_D[6]	1.58	1.61	1.59
A8	VO_E	3.20	3.23	3.21
A9	VO_D[0]	1.25	0.67	1.25
A10	VO_D[4]	1.58	1.62	1.60
A11	VO_D[8]	1.25	0.67	1.25
A12	VO_D[11]	1.08	0.94	1.06
A13	VO_D[14]	1.10	1.08	1.10
A14	AIN_MCLKI	NC	NC	NC
A15	AIN_MCLKO	3.22	3.23	3.20
A16	AOUT_IJC958	1.63	1.64	1.62
A17	AOUT_MCLKI	1.63	1.64	1.98
A18	AOUT_MCLKO	1.63	1.64	1.63
A19	A2OUT_D[0]	0.00	0.00	0.00
A20	UART2_TX	3.24	3.24	3.23
A21	SPI_CS1	0.00	0.00	0.00
A22	SPI_CS3	0.00	0.00	0.00
A23	SPI_CS2	0.00	0.00	0.00
A24	UART1_TX	3.23	3.24	3.22
A25	UART1_RX	2.31	2.32	2.30
A26	UART1_CTS	3.21	3.21	3.21
B1	VI_E[0]	3.21	3.22	3.21
B2	VI_D[0]	0.27	0.27	0.27
B3	VI_D[4]	1.39	1.39	1.39
B4	VI_D[7]	1.22	1.22	1.21
B5	VIO_D[0]	0.00	0.00	0.00
B6	VIO_D[3]	1.16	1.21	1.18
B7	VIO_D[7]	1.01	1.07	1.01
B8	VO_VSYNC	3.20	3.20	3.19
B9	VO_D[1]	1.18	1.22	1.18
B10	VO_D[5]	1.02	1.07	1.02
B11	VO_D[9]	1.19	1.22	1.18
B12	VO_D[12]	1.22	1.25	1.24
B13	VO_D[15]	2.17	2.14	2.17
B14	AIN_FSYNC	1.60	1.61	1.59
B15	A2_FSYNC	1.61	1.62	1.60
B16	AOUT_SCLK	1.62	1.62	1.61
B17	AIN_D[1]	0.00	0.00	0.00
B18	AOUT_D[2]	0.00	0.00	0.00
B19	UART2_CTS	4.91	4.91	4.91
B20	SDA	3.12	3.14	3.14
B21	SPI_CS0 --> SIO_SPI_CS0#	2.75	2.80	2.84
B22	SPI_MISO --> SIO_SPI_MISO	4.80	4.90	4.82
B23	SPI_CLK --> SIO_SPI_CLK	3.08	3.11	3.10
B24	UART1_RTS	3.21	3.21	3.21
B25	IRTX2	3.20	3.23	3.21
B26	IRRX	3.21	3.23	3.21
C1	VI_VSYNC[1]	2.24	2.25	2.25
C2	VI_D[1]	2.67	2.67	2.66
C3	VI_D[5]	1.32	1.32	1.32
C4	VI_D[8]	1.28	1.28	1.27
C5	VIO_D[1]	0.00	0.00	0.00
C6	VIO_D[4]	1.19	0.38	1.17
C7	VIO_D[8]	1.10	1.08	1.10
C8	VO_HSYNC	2.86	2.86	2.85
C9	VO_D[2]	1.18	0.38	1.18

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
C10	VO_D[6]	1.10	1.08	1.10
C11	VO_D[10]	1.19	0.38	1.17
C12	VO_D[13]	1.02	1.07	1.01
C13	AIN_SCLK	1.62	1.63	1.61
C14	A2IN_D_GPIO	0.00	0.00	0.00
C15	AOUT_FSYNC	1.62	1.63	1.61
C16	AIN_D[0]	1.21	1.21	1.20
C17	AOUT_D[3]	0.00	0.00	0.00
C18	AOUT_D[0]	1.62	1.64	1.61
C19	UART2_RTS	0.00	0.00	0.00
C20	SCL	3.15	3.18	3.16
C21	VDD_CORE	1.08	1.05	1.05
C22	VDD_CORE	1.08	1.05	1.05
C23	VDD_DRAM	2.35	2.29	2.30
C24	IRTX1	3.21	3.23	3.21
C25	SDRAM_A[2]	1.14	1.10	1.10
C26	SDRAM_A[3]	1.17	1.16	1.15
D1	TCK	2.25	2.25	2.25
D2	VI_D[2]	1.55	1.55	1.55
D3	VI_D[6]	1.50	1.50	1.49
D4	VI_D[9]	1.62	1.62	1.61
D5	VIO_D[2]	1.25	0.66	1.25
D6	VIO_D[5]	1.18	0.94	1.06
D7	VIO_D[9]	1.80	1.77	1.80
D8	VO_ACTIVE	2.49	2.49	2.48
D9	VO_D[3]	1.08	0.94	1.07
D10	VO_D[7]	1.81	1.78	1.81
D11	VDD_CORE	1.08	1.05	1.05
D12	VDD_CORE	1.08	1.05	1.05
D13	VDD_PAD1	3.22	3.24	3.22
D14	VDD_PAD2	3.22	3.24	3.22
D15	VDD_PAD3	3.22	3.24	3.22
D16	VDD_PAD4	3.22	3.24	3.22
D17	AOUT_D[1]	0.00	0.00	0.00
D18	A2_SCLK	1.61	1.61	1.60
D19	UART2_RX	4.91	4.91	4.91
D20	SPI_MOSI --> SIO_SPI_MOSI	3.05	3.05	3.04
D21	VDD_CORE	1.08	1.05	1.05
D22	SDRAM_VREF	1.19	1.17	1.17
D23	VDD_DRAM	2.35	2.29	2.30
D24	SDRAM_A[10]	1.12	1.08	1.04
D25	SDRAM_A[0]	1.14	1.09	1.03
D26	SDRAM_A[1]	1.14	1.09	1.08
E1	TDO	0.89	0.40	0.85
E2	TDI	2.23	2.24	2.24
E3	TMS	2.25	2.26	2.25
E4	TRSTn	0.00	0.00	0.00
E23	GND	0.00	0.00	0.00
E24	SDRAM_RASn	2.01	1.97	1.97
E25	SDRAM_BA[0]	1.21	1.18	1.18
E26	SDRAM_BA[1]	1.18	1.18	1.16
F1	AGND_AUDINPLL	0.00	0.00	0.00
F2	AGND_AUDOUTPLL	0.00	0.00	0.00
F3	AGND_SYSPLL	0.00	0.00	0.00
F4	BIAS_5V	1.05	1.05	1.06
F23	SDRAM_A[4]	1.19	1.16	1.15
F24	SDRAM_A[13]	1.18	1.06	1.02
F25	SDRAM_WEn	2.03	1.98	1.98
F26	SDRAM_CASn	2.08	1.93	1.85
G1	CLKI	1.48	1.49	1.49
G2	AGND_VIDPLL	0.00	0.00	0.00
G3	AVDD_AUDINPLL	1.05	1.05	1.06
G4	AVDD_SYSPLL	2.35	2.26	2.30
G23	SDRAM_A[8]	1.17	1.16	1.15
G24	SDRAM_A[7]	1.18	1.16	1.15
G25	SDRAM_A[6]	1.17	1.16	1.15

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
G26	SDRAM_A[5]	1.16	1.16	1.15
H1	CLKX	1.69	1.72	1.73
H2	AGND_DCXO	0.00	0.00	0.00
H3	AVDD33_DCXO	3.23	3.24	3.22
H4	AVDD_AUDOUTPLL	1.06	1.05	1.06
H23	SDRAM_CKE	2.10	2.05	2.05
H24	SDRAM_A[12]	1.14	1.09	1.06
H25	SDRAM_A[11]	1.12	1.08	1.05
H26	SDRAM_A[9]	1.17	1.14	1.15
J1	DAC_Dvss	0.00	0.00	0.00
J2	DAC_OUTB	1.58	1.58	1.58
J3	DAC_OUTB	1.58	1.58	1.58
J4	AVDD33_VIDPLL	3.23	3.23	3.22
J23	SDRAM_DQ[28]	1.18	1.18	1.18
J24	SDRAM_DQ[29]	1.11	1.11	1.11
J25	SDRAM_DQ[30]	1.11	1.11	1.11
J26	SDRAM_DQ[31]	1.11	1.11	1.11
K1	DAC2	0.63	0.61	0.64
K2	DAC1	0.64	0.62	0.64
K3	AVDD33_DAC	3.21	3.22	3.20
K4	VDD_CORE	1.08	1.05	1.05
K23	SDRAM_DQ[24]	1.11	1.11	1.11
K24	SDRAM_DQ[25]	1.13	1.13	1.13
K25	SDRAM_DQ[26]	1.12	1.12	1.12
K26	SDRAM_DQ[27]	1.11	1.11	1.11
L1	DAC5	0.72	0.72	0.72
L2	DAC3	0.73	0.73	0.64
L3	AVDD33_DAC	3.21	3.22	3.20
L4	VDD_CORE	1.08	1.05	1.05
L11	GND	0.00	0.00	0.00
L12	GND	0.00	0.00	0.00
L13	GND	0.00	0.00	0.00
L14	GND	0.00	0.00	0.00
L15	GND	0.00	0.00	0.00
L16	GND	0.00	0.00	0.00
L23	VDD_DRAM	2.35	2.29	2.30
L24	VDD_DRAM	2.35	2.29	2.30
L25	SDRAM_DQM[3]	0.35	0.32	0.30
L26	SDRAM_DQS[3]	1.16	1.16	1.15
M1	DAC6	0.72	0.72	0.73
M2	DAC4	0.64	0.62	0.73
M3	AVDD33_DACD	3.21	3.22	3.20
M4	VDD_PAD5	3.22	3.24	3.22
M11	GND	0.00	0.00	0.00
M12	GND	0.00	0.00	0.00
M13	GND	0.00	0.00	0.00
M14	GND	0.00	0.00	0.00
M15	GND	0.00	0.00	0.00
M16	GND	0.00	0.00	0.00
M23	SDRAM_CLK[1]	1.22	1.20	1.20
M24	VDD_DRAM	2.35	2.29	2.30
M25	SDRAM_DQM[2]	0.35	0.32	0.30
M26	SDRAM_DQS[2]	1.16	1.16	1.15
N1	GND_BATT	0.00	0.00	0.00
N2	VSS_REF	0.00	0.00	0.00
N3	RTC_CLKI	0.00	0.00	0.00
N4	VDD_PAD6	3.22	3.24	3.22
N11	GND	0.00	0.00	0.00
N12	GND	0.00	0.00	0.00
N13	GND	0.00	0.00	0.00
N14	GND	0.00	0.00	0.00
N15	GND	0.00	0.00	0.00
N16	GND	0.00	0.00	0.00
N23	SDRAM_CLKn[1]	1.20	1.17	1.16
N24	VDD_DRAM	2.35	2.29	2.30
N25	SDRAM_DQ[22]	1.13	1.13	1.13
N26	SDRAM_DQ[23]	1.13	1.13	1.13

PIN NO.	PIN NAME	EE MODE	PB MODE	REC MODE
P1	V_REF	1.18	1.18	1.18
P2	VDD_REF	3.22	3.23	3.22
P3	RTC_CLKX	NC	NC	NC
P4	VDD_PAD7	3.22	3.24	3.22
P11	GND	0.00	0.00	0.00
P12	GND	0.00	0.00	0.00
P13	GND	0.00	0.00	0.00
P14	GND	0.00	0.00	0.00
P15	GND	0.00	0.00	0.00
P16	GND	0.00	0.00	0.00
P23	SDRAM_CLK[0]	1.21	1.19	1.19
P24	VDD_DRAM	2.35	2.29	2.30
P25	SDRAM_DQ[20]	1.13	1.13	1.13
P26	SDRAM_DQ[21]	1.14	1.14	1.14
R1	AGND_ADCD	0.00	0.00	0.00
R2	AVDD33_ADCD	0.00	0.00	0.00
R3	VDD_BATT	0.00	0.00	0.00
R4	VDD_PAD8	3.22	3.24	3.22
R11	GND	0.00	0.00	0.00
R12	GND	0.00	0.00	0.00
R13	GND	0.00	0.00	0.00
R14	GND	0.00	0.00	0.00
R15	GND	0.00	0.00	0.00
R16	GND	0.00	0.00	0.00
R23	SDRAM_CLKn[0]	1.20		

5. ALUMINUM CAPACITORS on MAIN BOARD

Location No.	Capacity	Capacitor Voltage Spec	EE Mode	Playback Mode	Record Mode
C1152	100uF	16	4.95	4.95	4.95
C1153	100uF	16	2.48	2.48	2.48
C1233	220uF	6	1.21	1.21	1.2
C1281	220uF	6	1.21	1.21	1.2
C1282	220uF	6	2.4	2.4	2.4
C1285	220uF	6	2.4	2.4	2.4
C1286	220uF	6	2.4	2.4	2.4
C1403	220uF	6	3.26	3.26	3.26
C1404	220uF	6	3.27	3.27	3.27
C1407	220uF	6	4.95	4.95	4.95
C1408	220uF	6	1.8	1.8	1.79
C1410	220uF	6	1.23	1.23	1.23
C1413	100uF	16	4.95	4.95	4.95

INFORMATION :

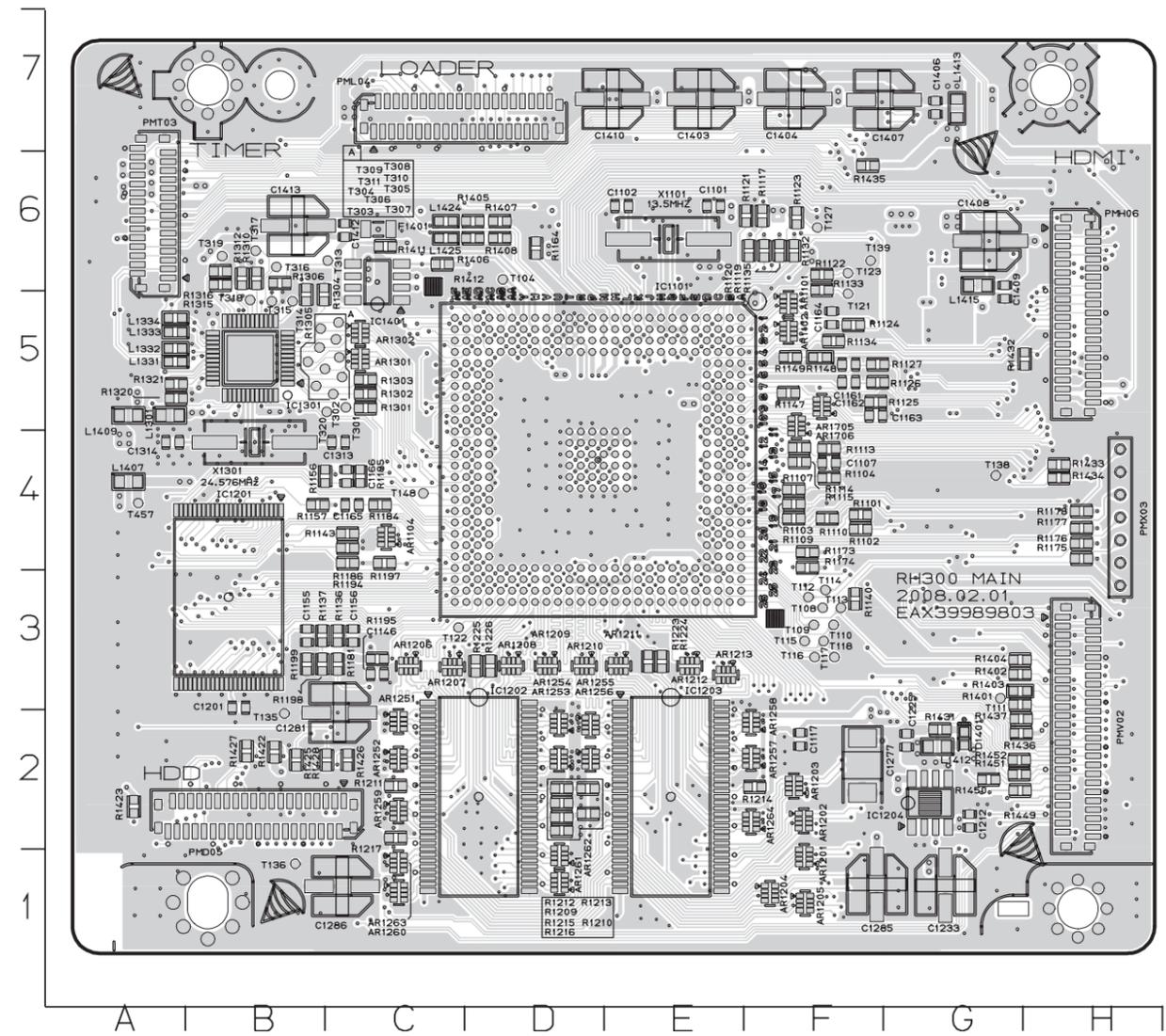
1. Voltage Check using RH 300 DV1
2. SET : Ver=070827B Cware=v15_06 BSP=rh3t FME
IO : Ver=70824_1 Loader: S603
3. EE Mode : Check with Signal C2
4. Playback Mode : Check with DVD TEST DISC KDV-N Chapter 2
5. Record Mode : Check with recording signal C2 using DVD -RW
Brand : Mitsubishi, VR Mode

6. CAPACITORS on I/O BOARD

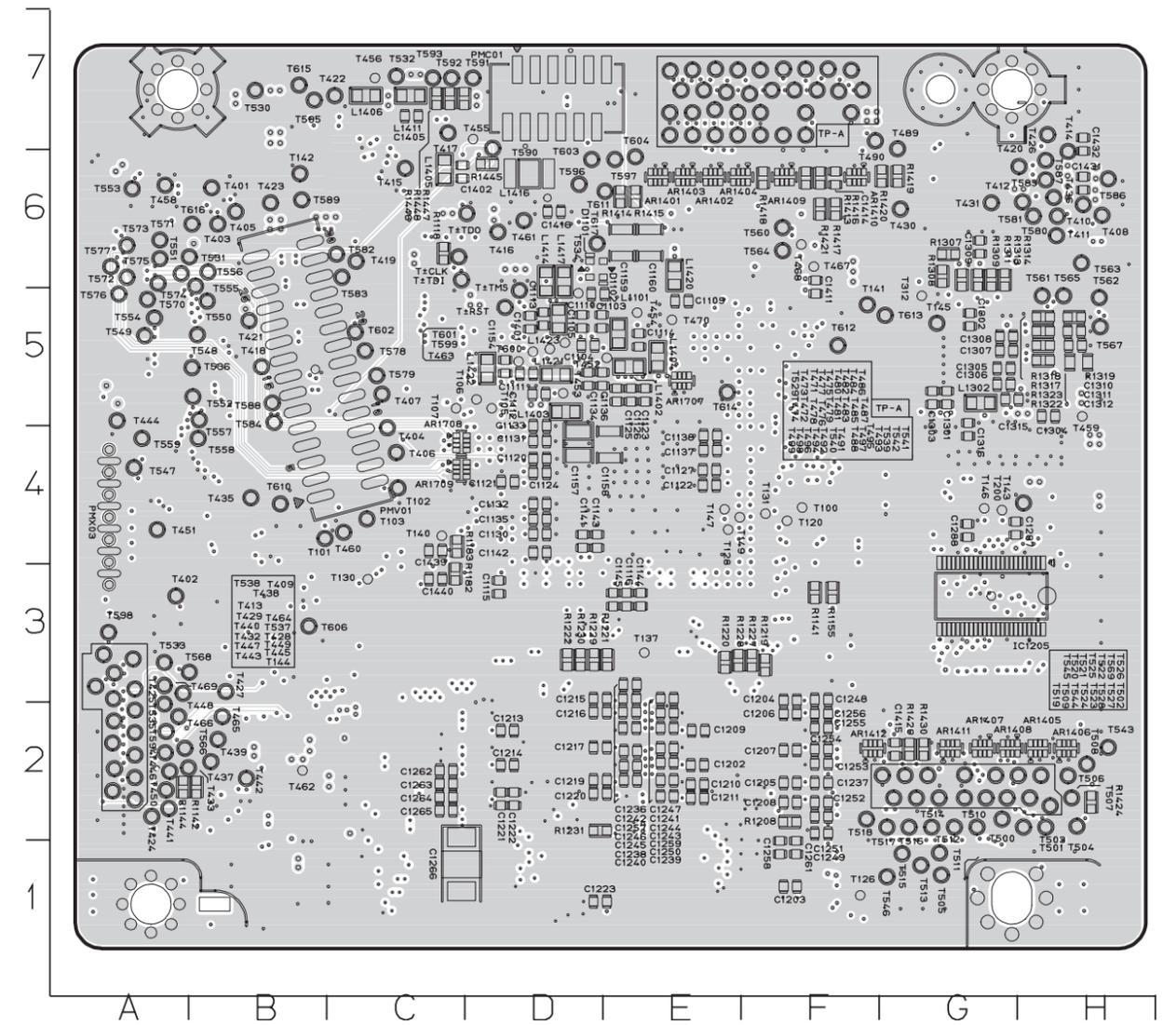
Loca. No.	Value Capacitor	EE Mode				Playback				Record				
		Voltage_Spec	Positive (+)	Negative (-)	Gap	Margin	Positive (+)	Negative (-)	Gap	Margin	Positive (+)	Negative (-)	Gap	Margin
C152	100uF	16V	3.12V	0V	3.12V	12.88V	3.12V	0V	3.12V	12.88V	3.1V	0V	3.1V	12.9V
C164	100uF	16V	2.5V	0V	2.5V	13.5V	2.51V	0V	2.51V	13.49V	2.47V	0V	2.47V	13.53V
C165	100uF	16V	3.31V	0V	3.31V	12.69V	3.31V	0V	3.31V	12.69V	3.3V	0V	3.3V	12.7V
C163	47uF	16V	5.22V	0V	5.22V	10.78V	5.22V	0V	5.22V	10.78V	5.2V	0V	5.2V	10.8V
C162	4.7uF	50V	12.64V	0V	12.64V	37.36V	12.62V	0V	12.62V	37.38V	12.66V	0V	12.66V	37.34V
C159	100uF	16V	1.81V	0V	1.81V	14.19V	1.81V	0V	1.81V	14.19V	1.79V	0V	1.79V	14.21V
C602	10uF	16V	2.34V	0V	2.34V	15.37V	2.34V	0V	2.34V	15.37V	2.34V	0V	2.34V	13.66V
C603	220uF	6.3V	2.34V	1.31V	1.03V	5.27V	2.33V	1.31V	1.02V	5.28V	2.34V	1.33V	1.01V	5.29V
C618	22uF	16V	5.19V	0V	5.19V	10.81V	5.19V	0V	5.19V	10.81V	5.17V	0V	5.17V	10.83V
C624	470uF	10V	4.83V	0V	4.83V	5.17V	4.83V	0V	4.83V	5.17V	4.8V	0V	4.8V	5.2V
C632	22uF	16V	1.8V	0V	1.8V	14.2V	1.81V	0V	1.81V	14.19V	1.78V	0V	1.78V	14.22V
C634	22uF	16V	3.23V	0V	3.23V	12.77V	3.22V	0V	3.22V	12.78V	3.2V	0V	3.2V	12.8V
C807	22uF	16V	12V	0V	12V	4V	11.99V	0V	11.99V	4.01V	12V	0V	12V	4V
C808	22uF	16V	6V	2.44V	3.56V	12.44V	6V	2.43V	3.57V	12.43V	6V	2.4V	3.6V	12.4V
C823	10uF	16V	6V	0V	6V	10V	6V	0V	6V	10V	6V	0V	6V	10V
C829	22uF	16V	6V	2.4V	3.6V	12.4V	6V	2.4V	3.6V	12.4V	6V	2.41V	3.59V	12.41V
C843	22uF	16V	6V	0V	6V	10V	6V	0V	6V	10V	6V	0V	6V	10V
C844	22uF	16V	6V	0V	6V	10V	6V	0V	6V	10V	6V	0V	6V	10V
C858	22uF	16V	6.48V	1.92V	4.56V	11.44V	6.48V	1.92V	4.56V	11.44V	6.46V	1.93V	4.53V	11.47V
C859	22uF	16V	1.6V	1.8V	-0.2V	16.2V	1.6V	1.8V	-0.2V	16.2V	1.6V	1.8V	-0.2V	16.2V
C875	22uF	16V	6.49V	1.96V	4.53V	11.47V	6.48V	1.98V	4.5V	11.5V	6.46V	2.05V	4.41V	11.59V
C868	22uF	16V	11.99V	0V	11.99V	4.01V	11.99V	0V	11.99V	4.01V	12.01V	0V	12.01V	3.99V
C849	22uF	16V	1.48V	43V	-41.52V	57.52V	1.59V	0.54V	1.05V	14.95V	1.48V	0.44V	1.04V	14.96V
C867	22uF	16V	2.49V	0V	2.49V	13.51V	2.49V	0V	2.49V	13.51V	2.46V	0V	2.46V	13.54V
C825	22uF	16V	6.49V	0V	6.49V	9.51V	6.49V	0V	6.49V	9.51V	6.46V	0V	6.46V	9.54V
C826	22uF	16V	1.61V	0V	1.61V	14.39V	1.61V	0V	1.61V	14.39V	1.61V	0V	1.61V	14.39V
C845	22uF	16V	6.49V	0V	6.49V	9.51V	6.49V	0V	6.49V	9.51V	6.46V	0V	6.46V	9.54V
C872	470uF	10V	1.93V	0.14V	1.79V	8.21V	1.9V	0.21V	1.69V	8.31V	1.96V	0.07V	1.89V	8.11V
C876	470uF	10V	1.94V	0V	1.94V	8.06V	2.27V	0V	2.27V	7.73V	1.96V	0V	1.96V	8.04V
C848	220uF	6.3V	2.53V	2.42V	0.11V	6.19V	2.54V	2.42V	0.12V	6.18V	2.51V	2.41V	0.1V	6.2V
C870	22uF	16V	5.18V	0V	5.18V	10.82V	5.18V	0V	5.18V	10.82V	5.16V	0V	5.16V	10.84V
C871	470uF	10V	1.97V	0V	1.97V	8.03V	1.95V	0V	1.95V	8.05V	1.99V	0V	1.99V	8.01V
C873	220uF	6.3V	2.53V	0V	2.53V	3.77V	2.53V	0V	2.53V	3.77V	2.52V	0V	2.52V	3.78V
C874	220uF	6.3V	2.53V	0V	2.53V	3.77V	2.53V	0V	2.53V	3.77V	2.52V	0V	2.52V	3.78V
C850	470uF	10V	1.93V	1.92V	0.01V	9.99V	1.95V	1.9V	0.05V	9.95V	1.95V	1.92V	0.03V	9.97V
C706	470uF	10V	5.21V	0V	5.21V	4.79V	5.21V	0V	5.21V	4.79V	5.19V	0V	5.19V	4.81V
C709	47uF	16V	5.21V	0V	5.21V	10.79V	5.21V	0V	5.21V	10.79V	5.19V	0V	5.19V	10.81V
C903	10uF	16V	3.21V	0V	3.21V	12.79V	3.21V	0V	3.21V	12.79V	3.2V	0V	3.2V	12.8V
C904	10uF	16V	1.8V	0V	1.8V	14.2V	1.8V	0V	1.8V	14.2V	1.77V	0V	1.77V	14.23V
C906	10uF	16V	1.6V	0V	1.6V	14.4V	1.6V	0V	1.6V	14.4V	1.58V	0V	1.58V	14.42V
C950	22uF	16V	6.48V	1.6V	4.88V	11.12V	6.47V	1.6V	4.87V	11.13V	6.45V	1.58V	4.87V	11.13V
C951	22uF	16V	6.48V	1.6V	4.88V	11.12V	6.48V	1.6V	4.88V	11.12V	6.45V	1.58V	4.87V	11.13V
C952	10uF	16V	3.26V	0V	3.26V	12.74V	3.26V	0V	3.26V	12.74V	3.24V	0V	3.24V	12.76V
C909	47uF	16V	1.61V	0V	1.61V	14.39V	1.61V	0V	1.61V	14.39V	1.59V	0V	1.59V	14.41V
C955	10uF	16V	3.26V	0V	3.26V	12.74V	3.26V	0V	3.26V	12.74V	3.24V	0V	3.24V	12.76V
C943	22uF	16V	7.07V	1.62V	5.45V	10.55V	7.05V	1.62V	5.43V	10.57V	7.04V	1.61V	5.43V	10.57V
C944	22uF	16V	7.07V	1.62V	5.45V	10.55V	7.07V	1.62V	5.45V	10.55V	7.04V	1.61V	5.43V	10.57V
C948	10uF	16V	3.26V	0V	3.26V	12.74V	3.25V	0V	3.25V	12.75V	3.24V	0V	3.24V	12.76V

PRINTED CIRCUIT BOARD DIAGRAMS

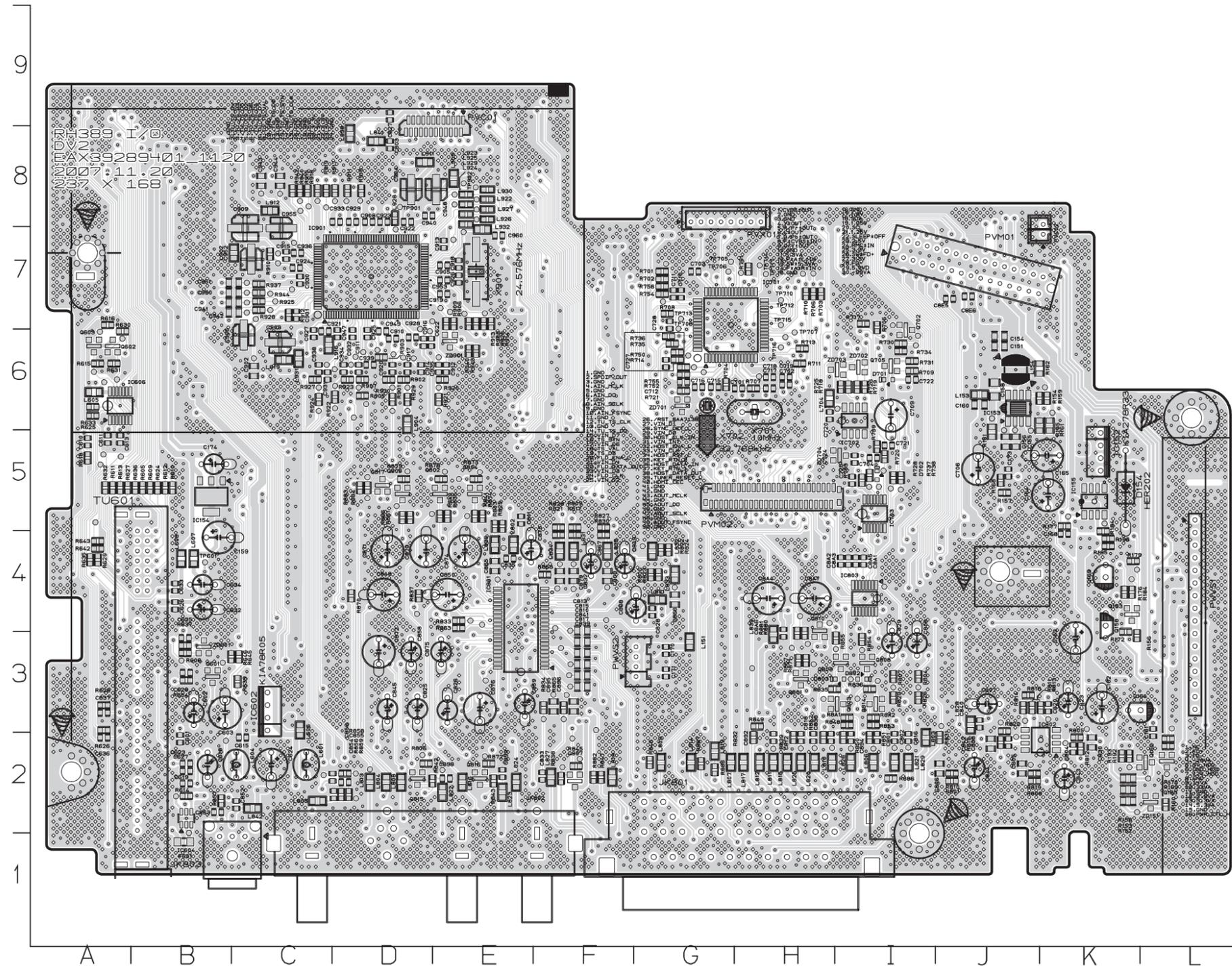
1. MAIN P.C.BOARD (TOP VIEW)



(BOTTOM VIEW)



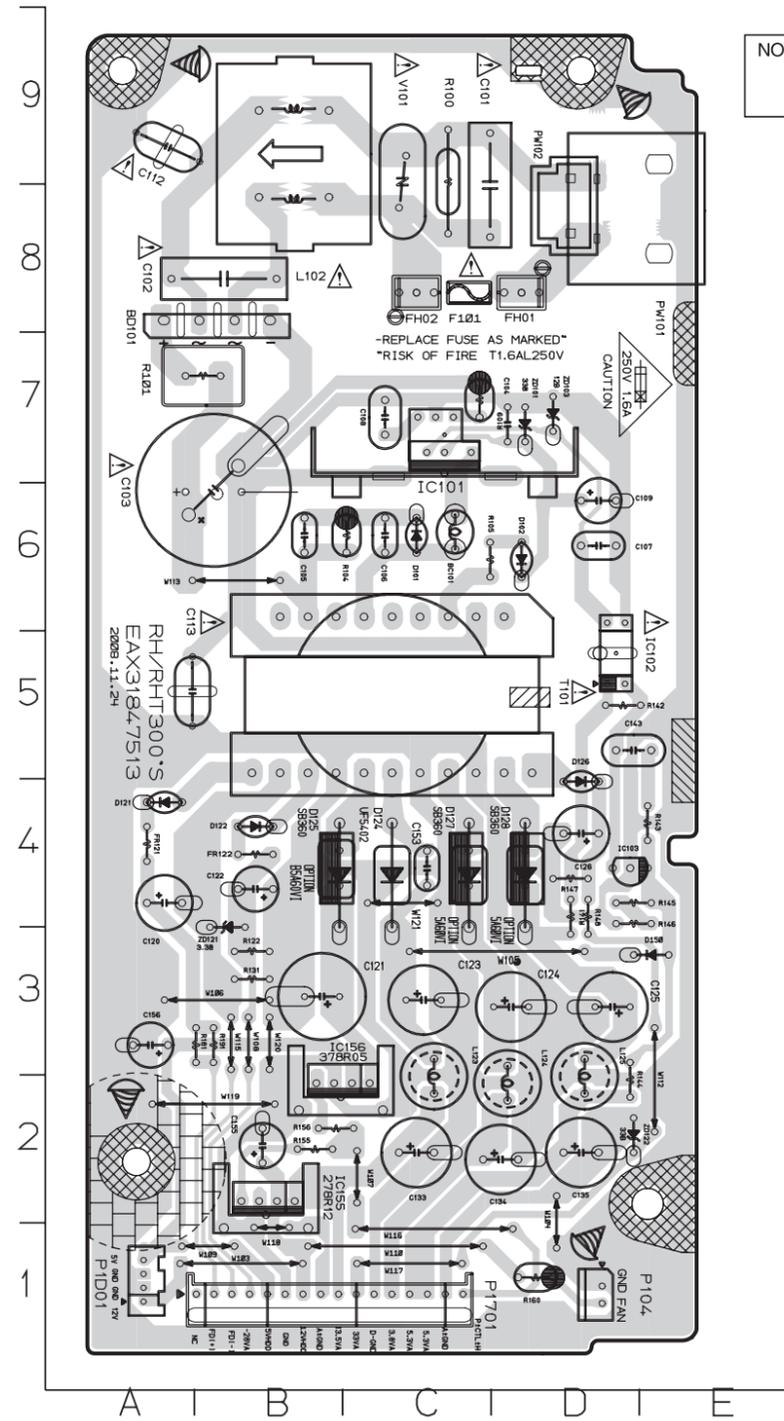
**2. I/O P.C.BOARD
(TOP VIEW)**



I/O P.C.BOARD
(BOTTOM VIEW)

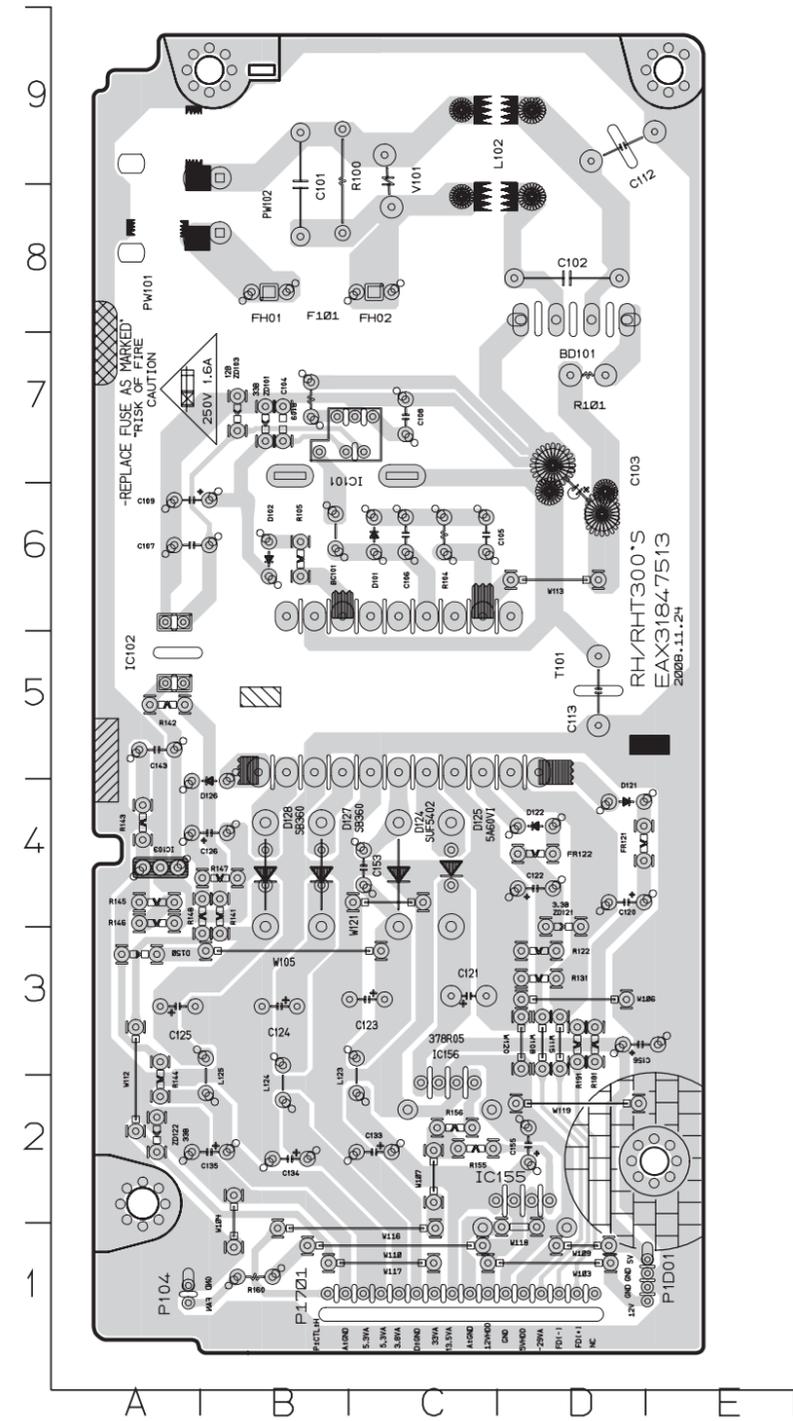


3. SMPS P.C.BOARD (TOP VIEW)

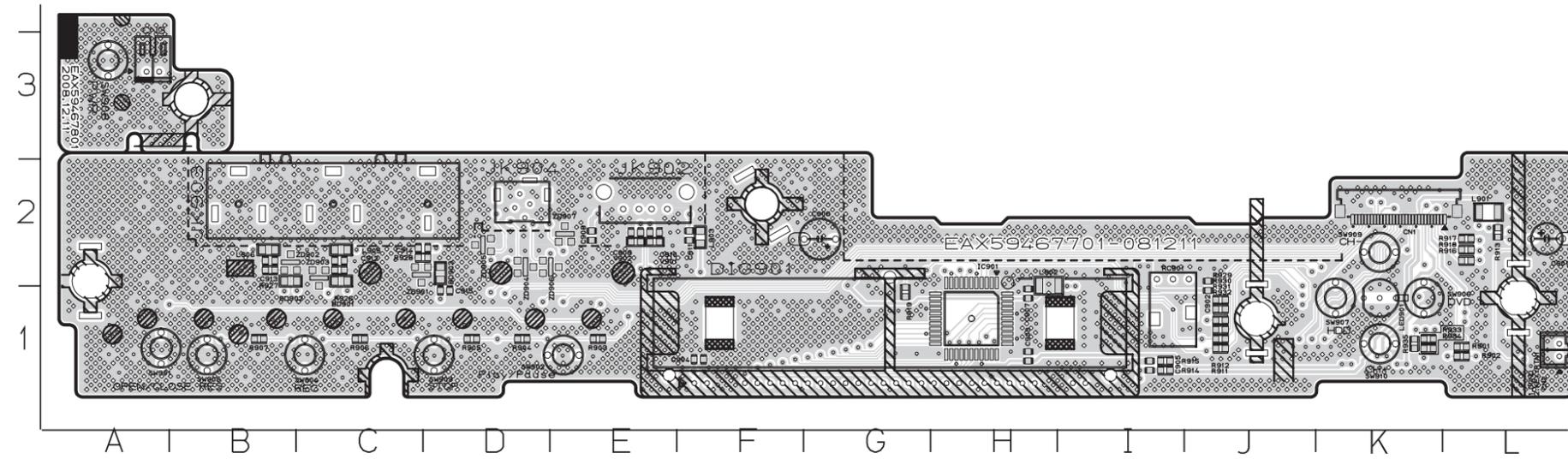


NOTE) ⚠ Warning
Parts that are shaded are critical
with respect to risk of fire or
electrical shock.

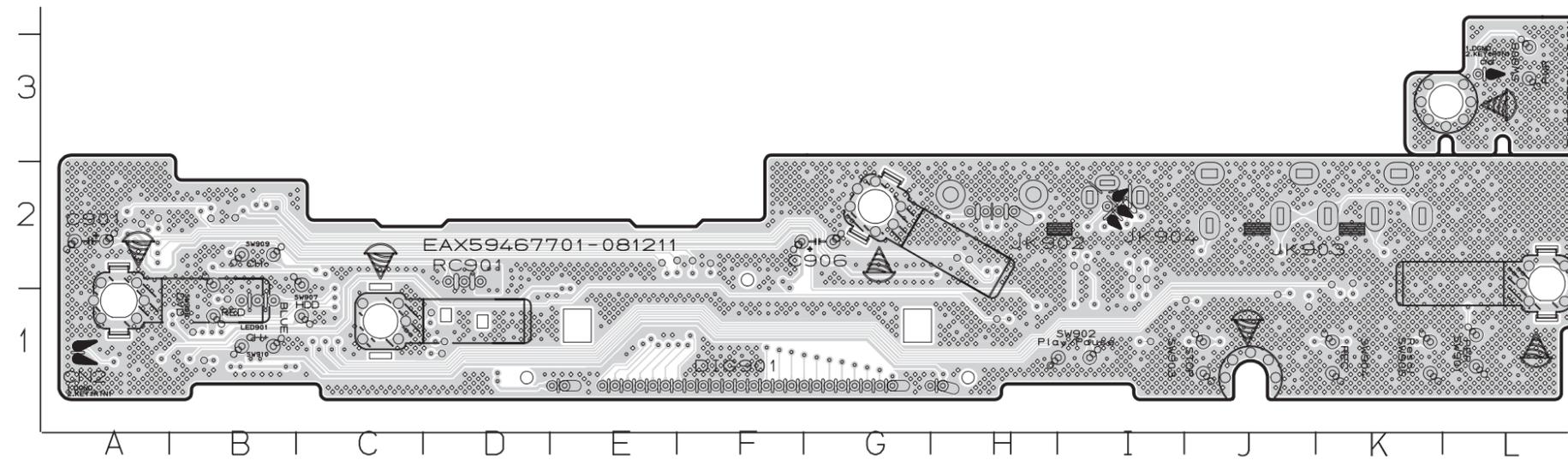
(BOTTOM VIEW)



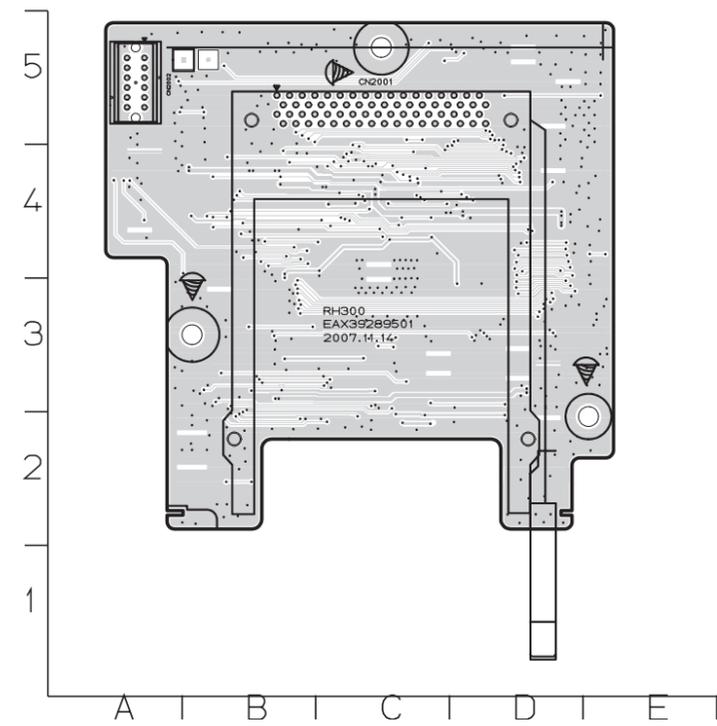
**4. TIMER & KEY P.C.BOARD
(TOP VIEW)**



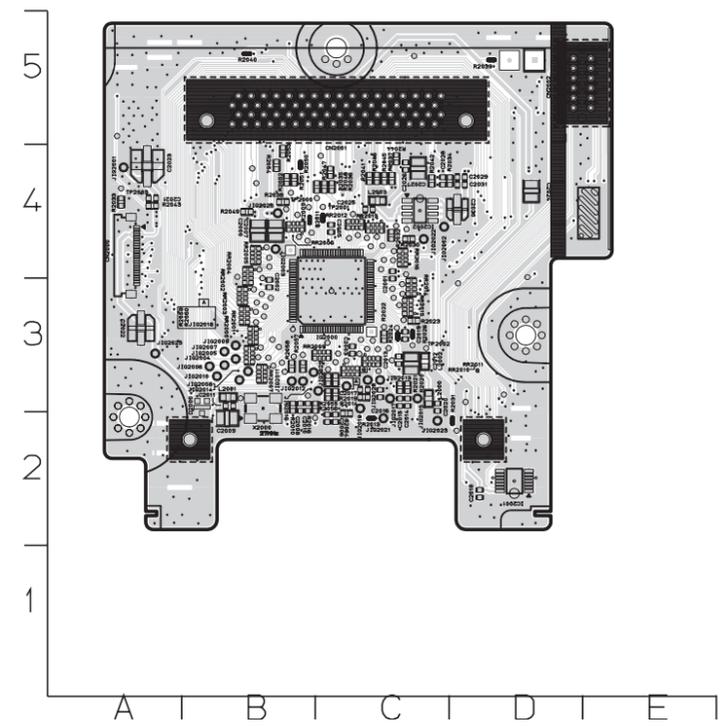
(BOTTOM VIEW)



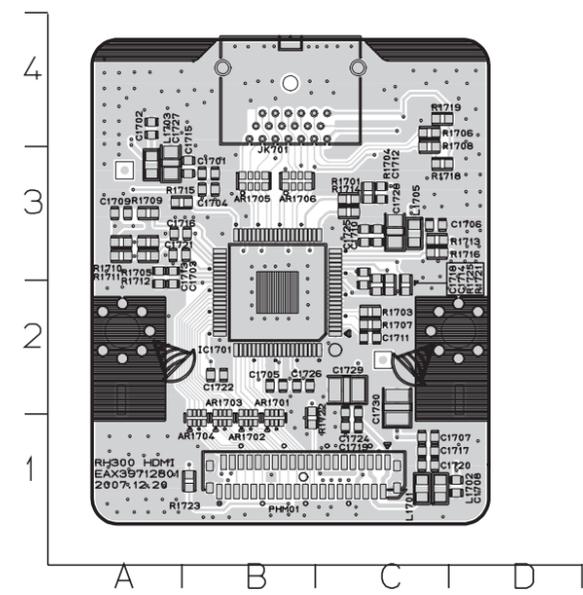
5. COMMON INTERFACE P.C.BOARD(OPTIONAL)
(TOP VIEW)



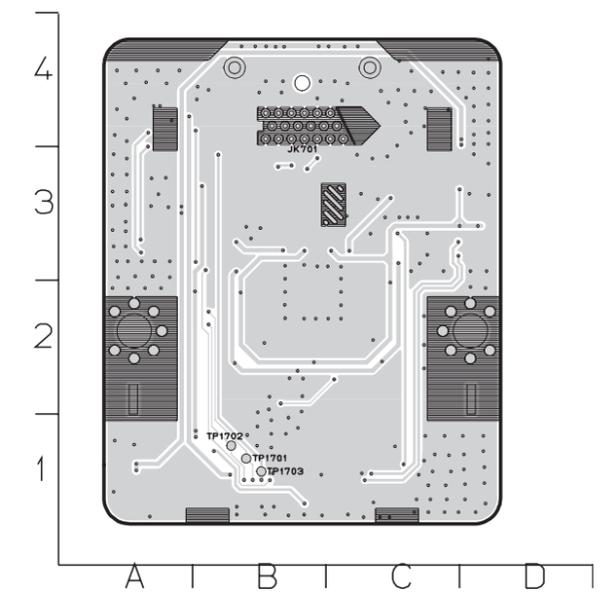
(BOTTOM VIEW)



6. HDMI P.C.BOARD
(TOP VIEW)



(BOTTOM VIEW)



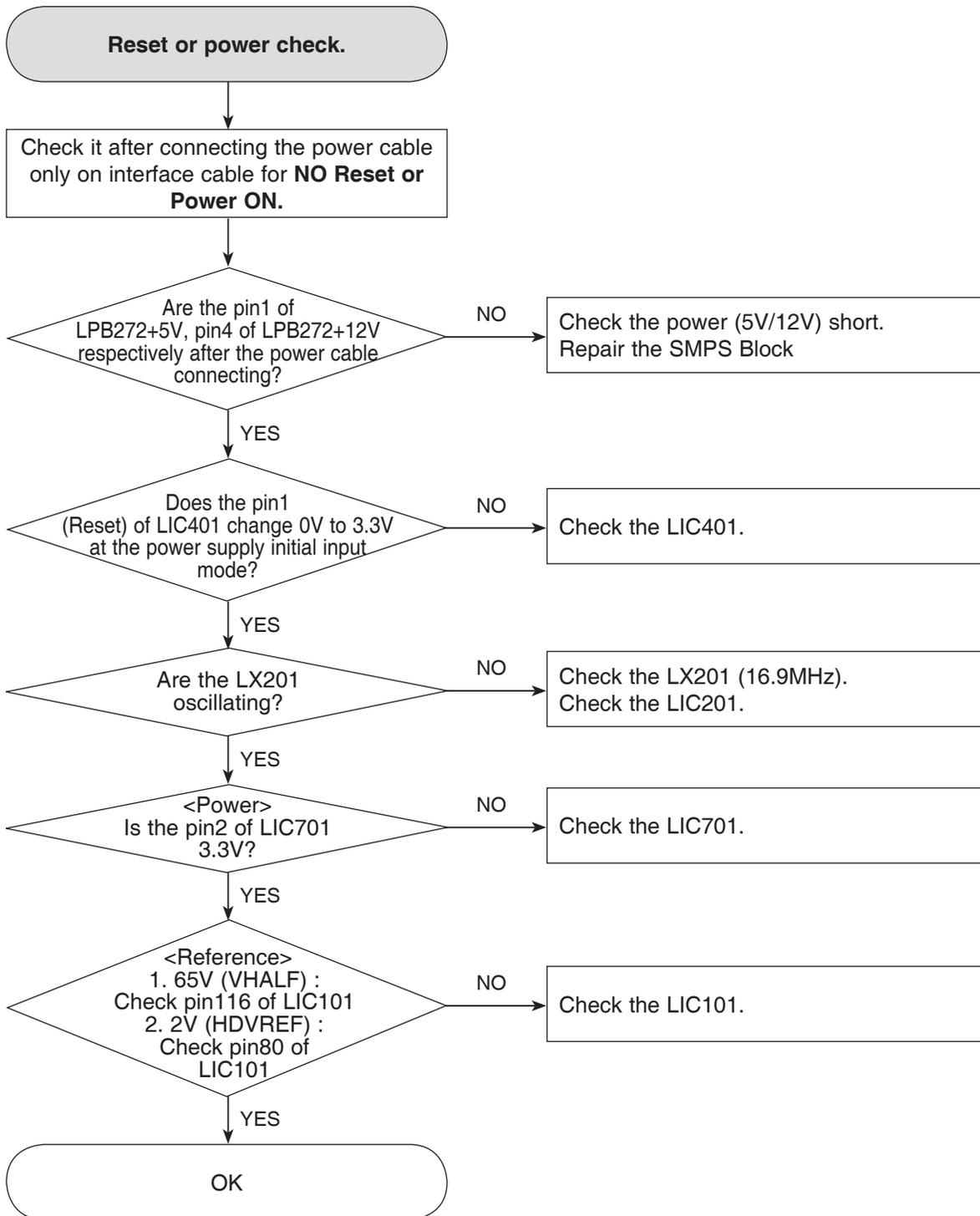
SECTION 4

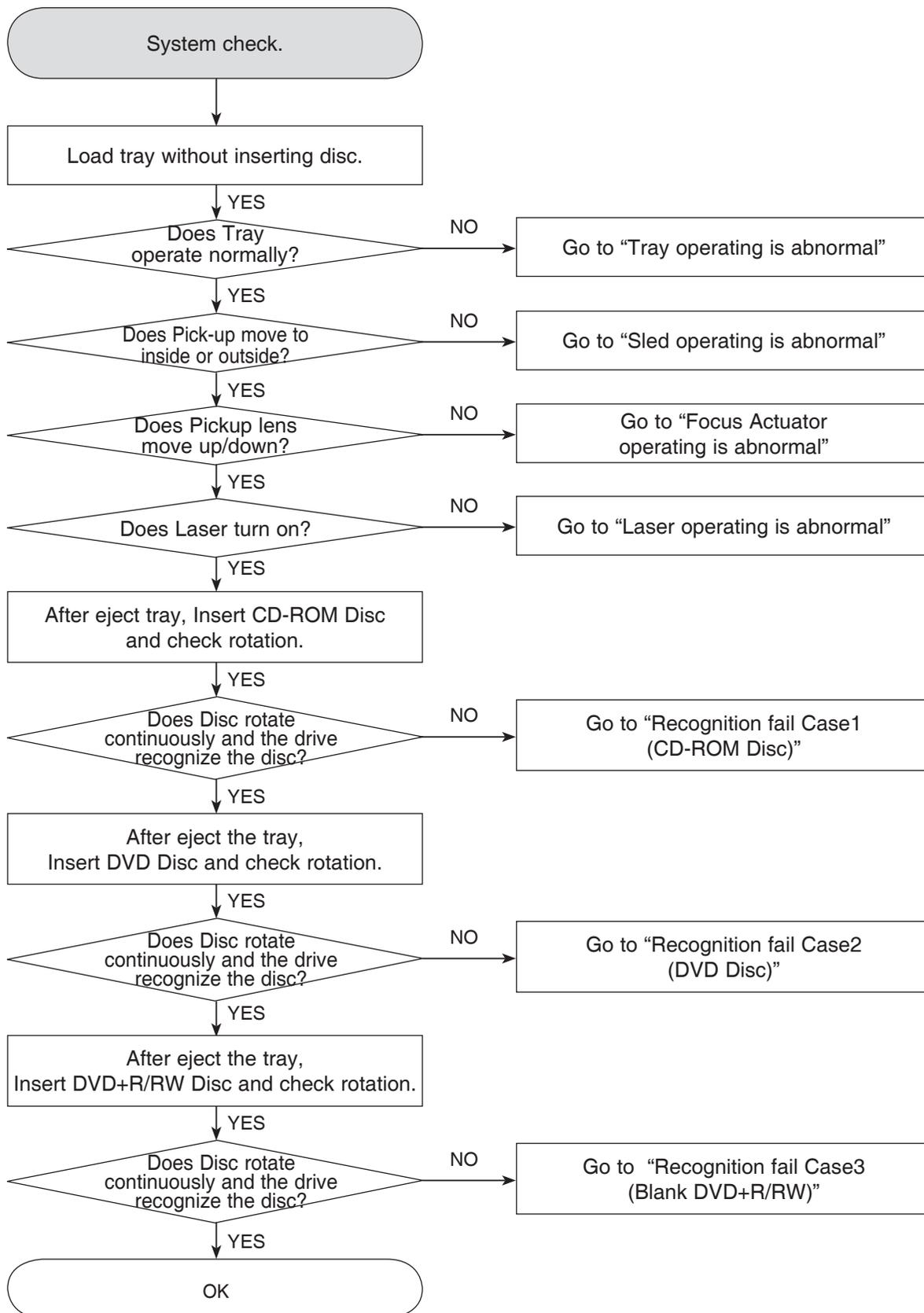
RS-06A LOADER PART

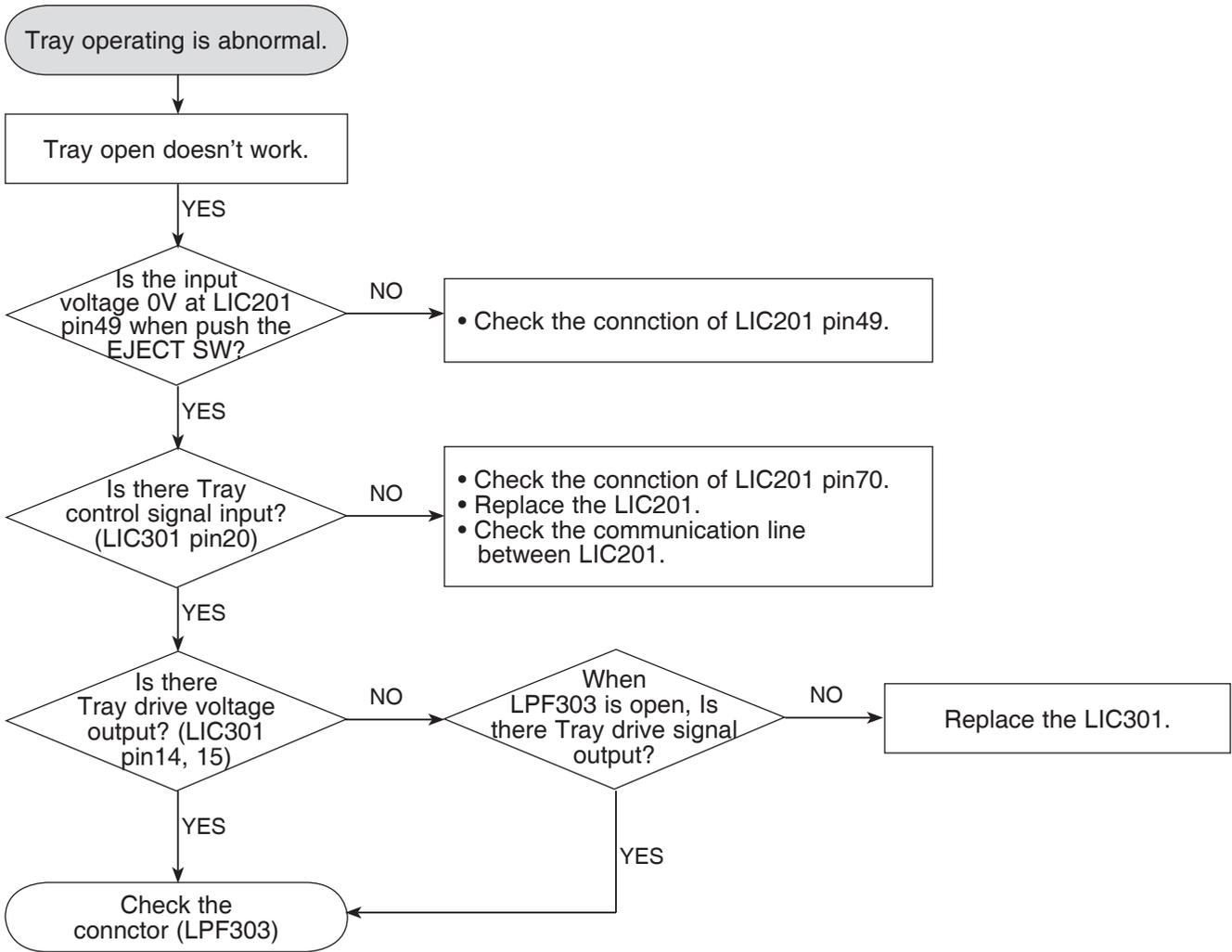
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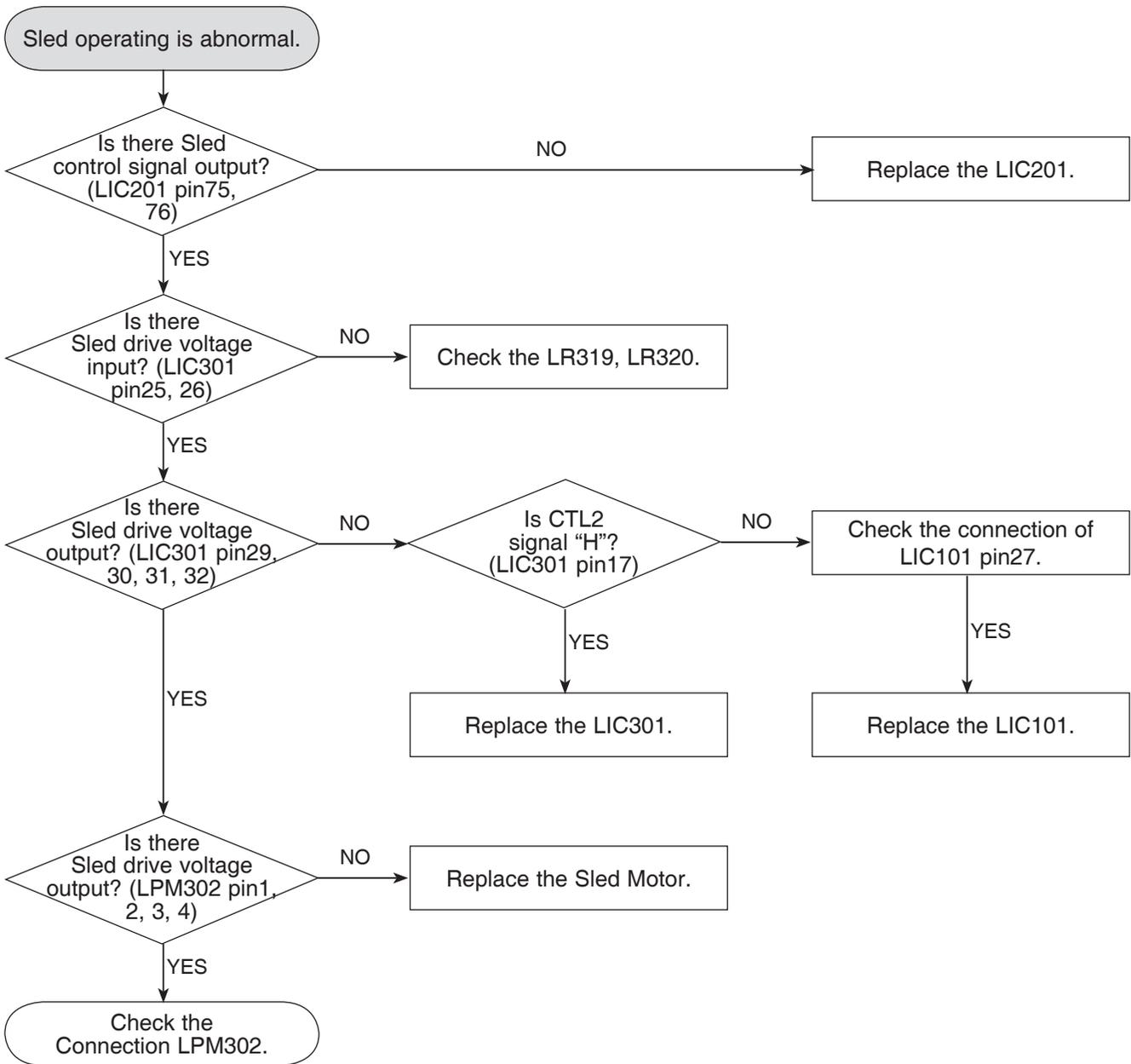
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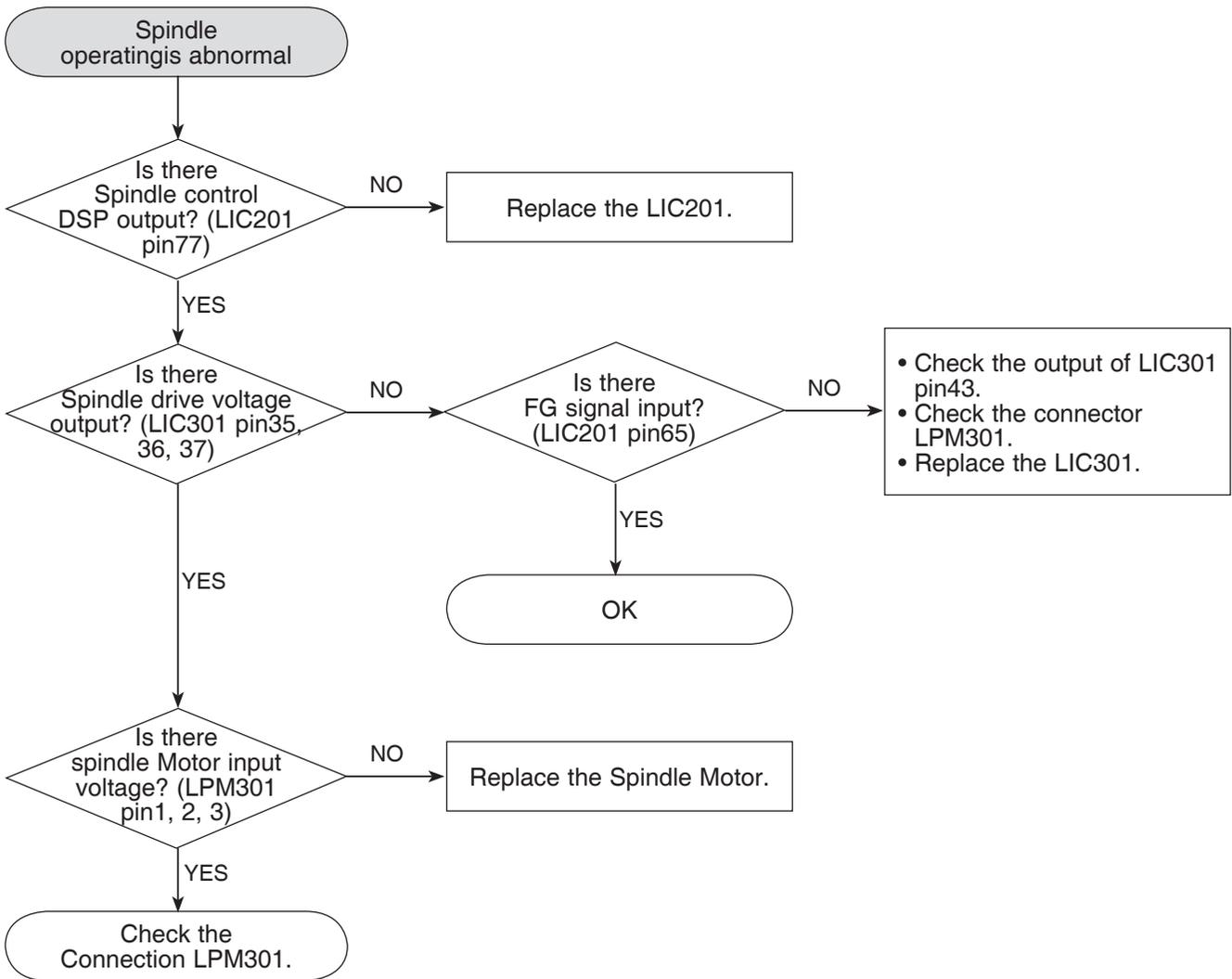
ELECTRICAL TROUBLESHOOTING GUIDE

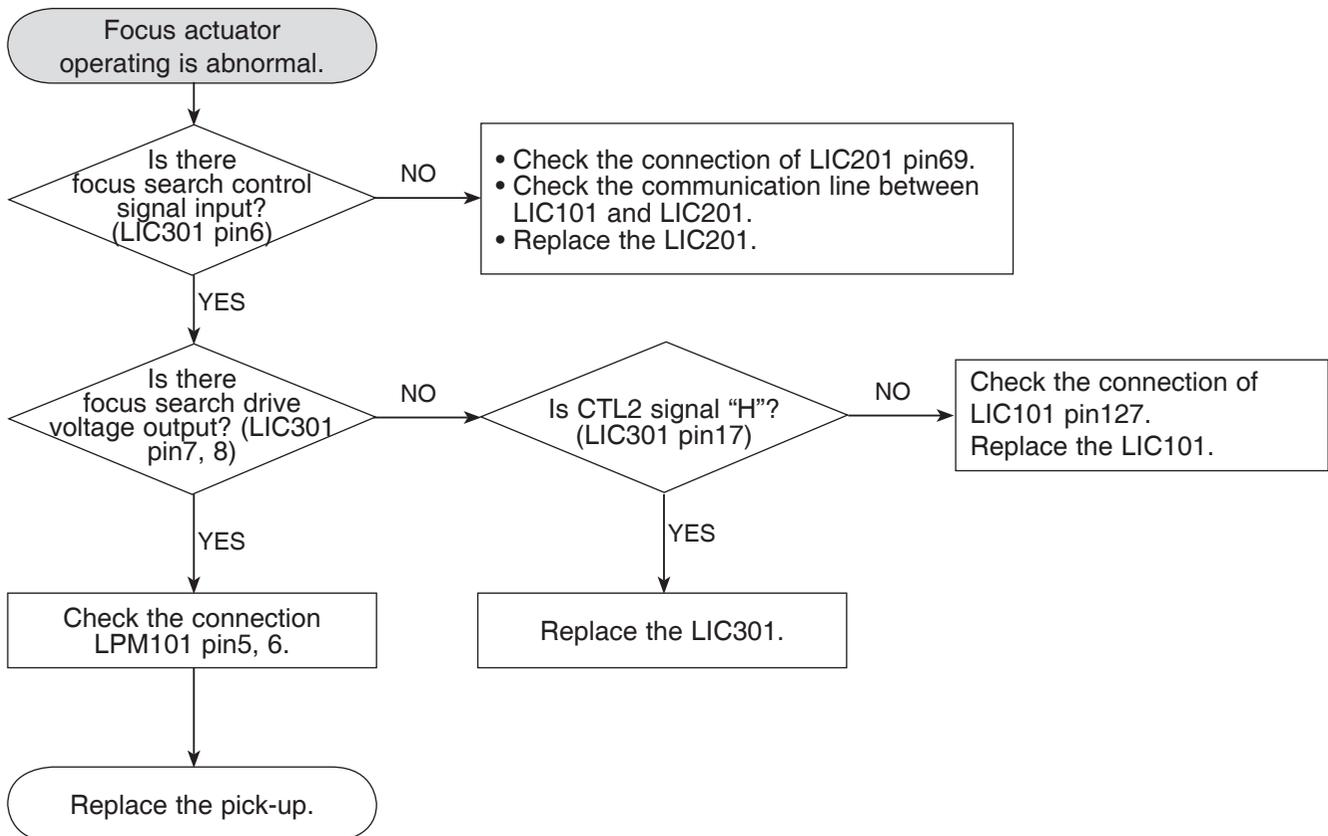
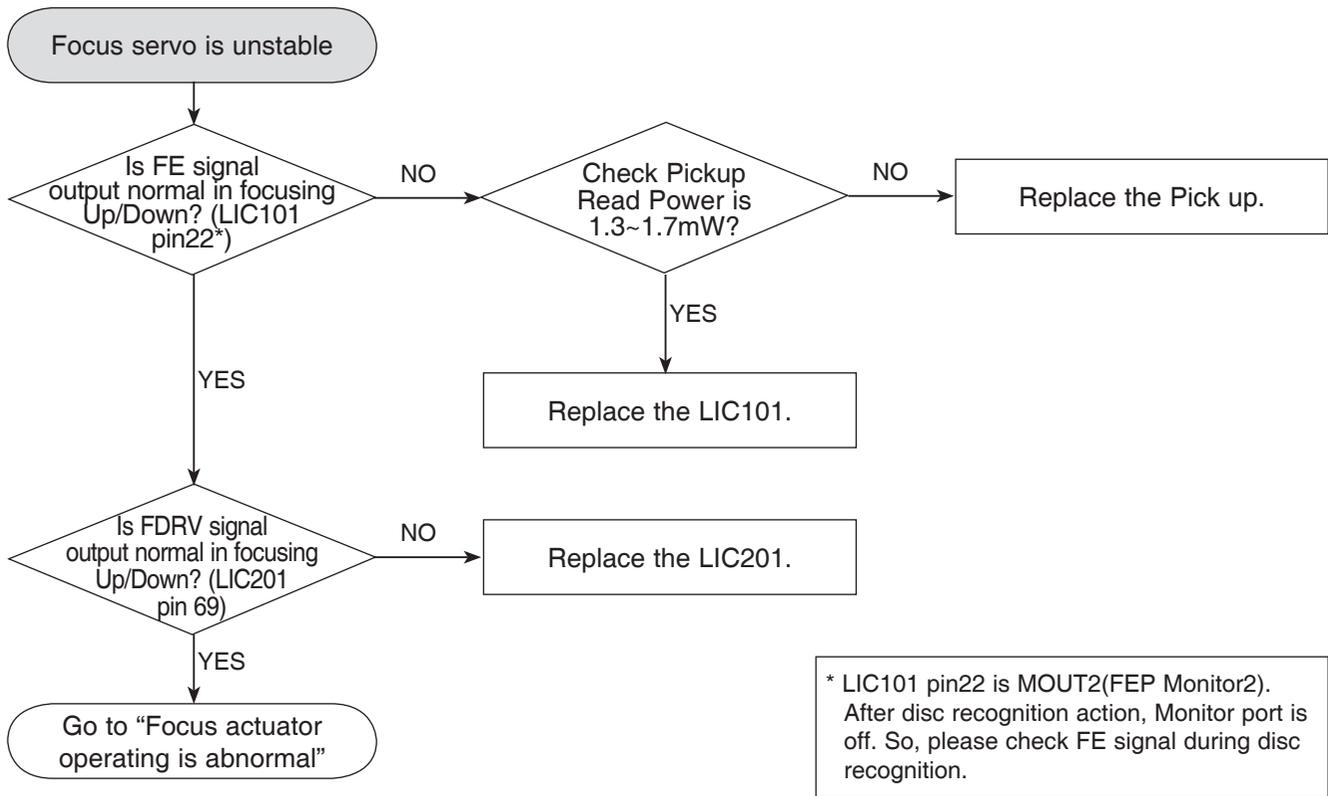


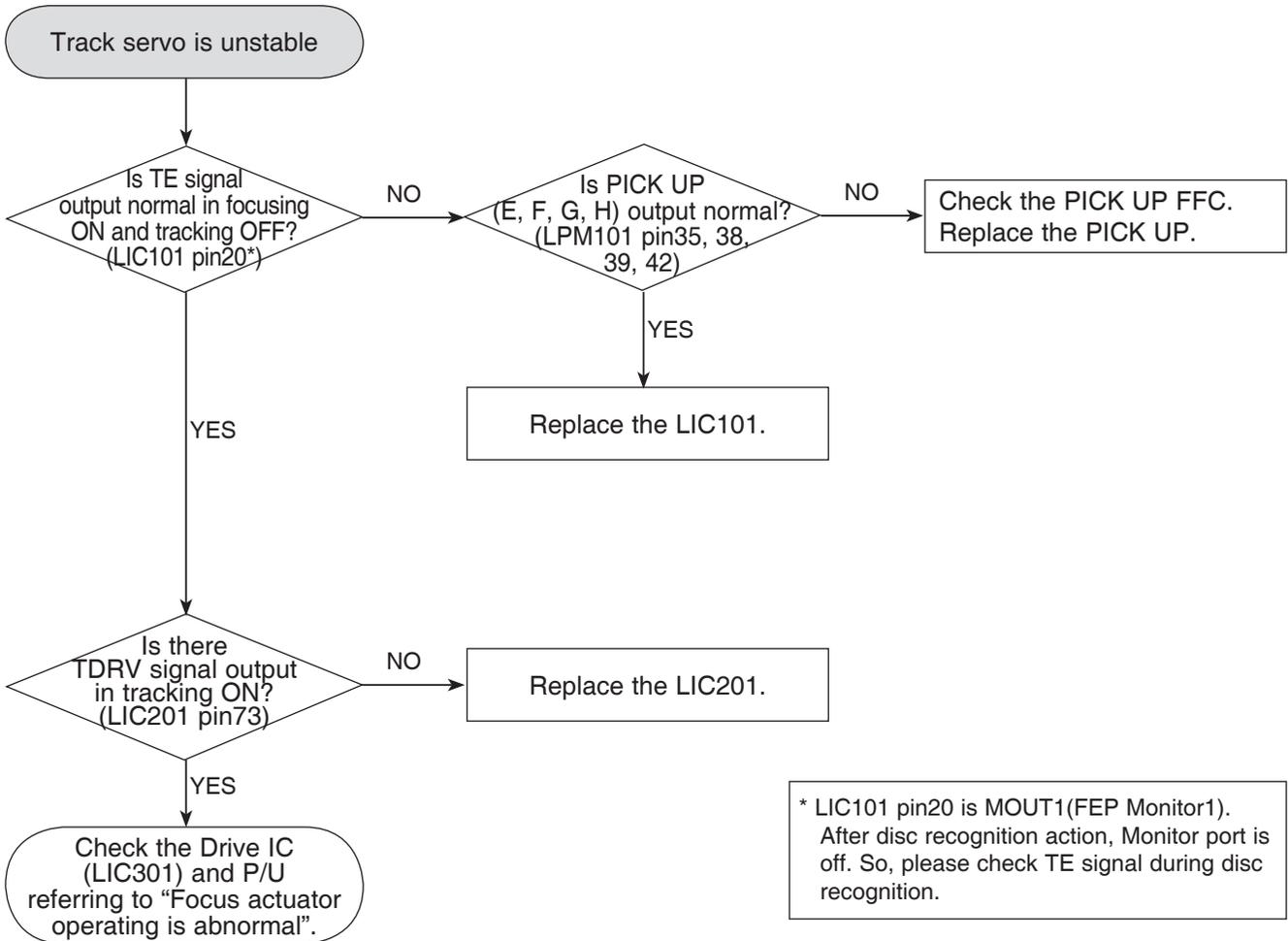




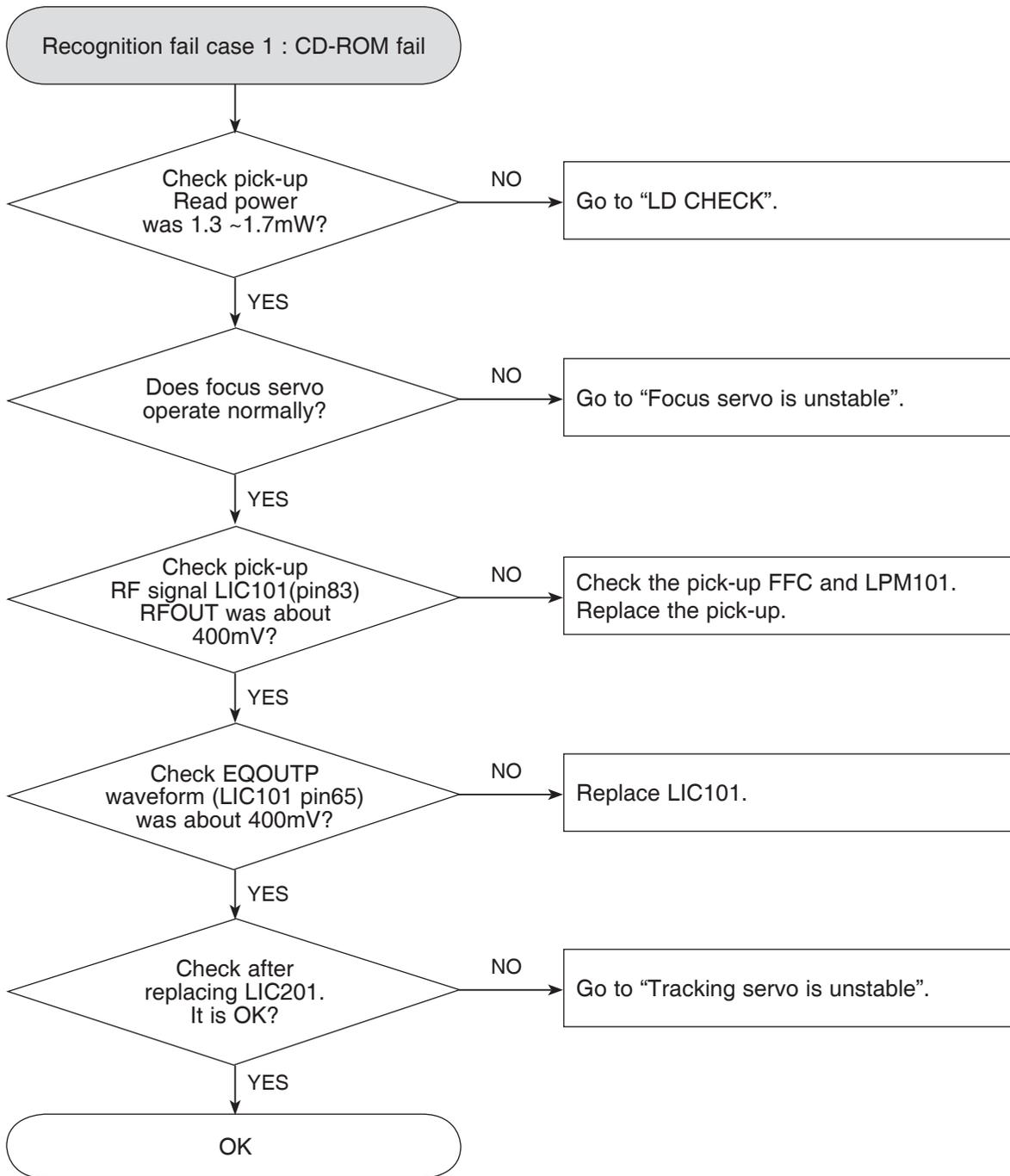


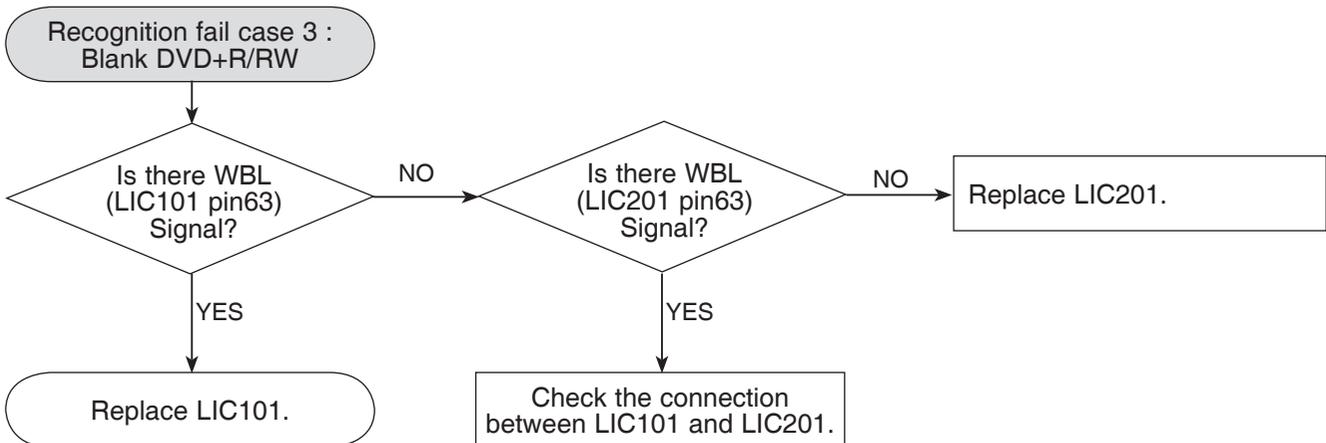
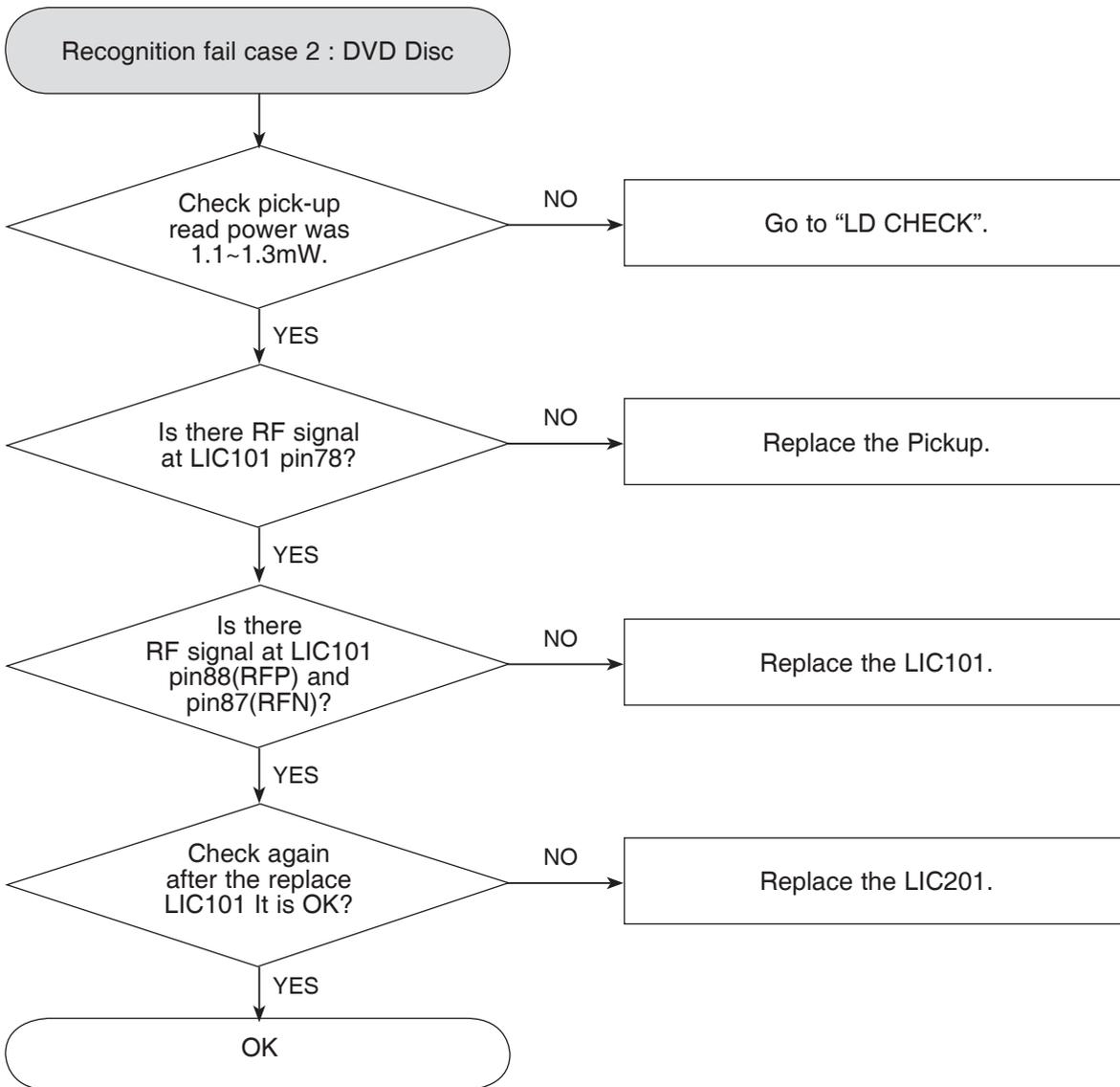


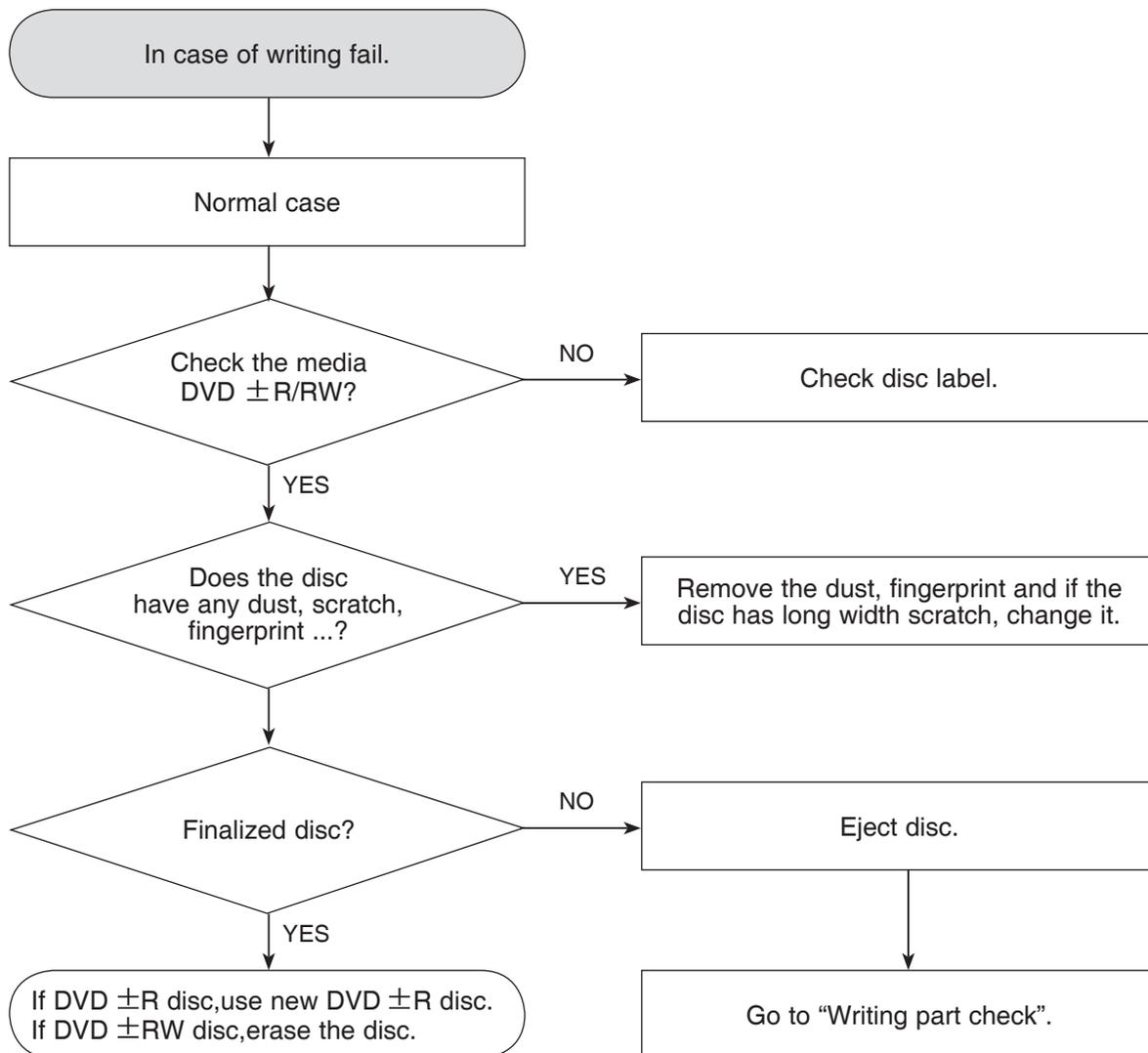


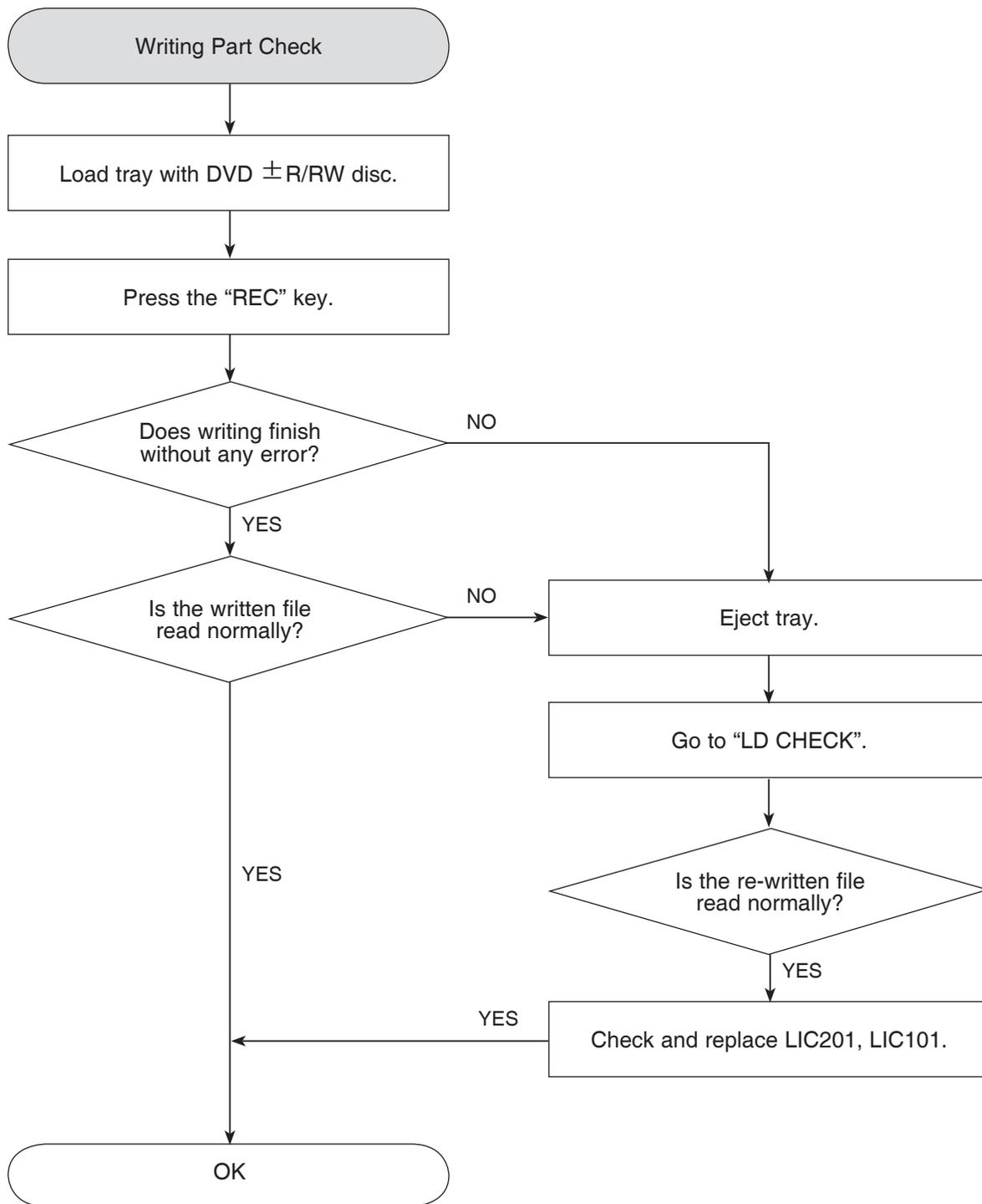


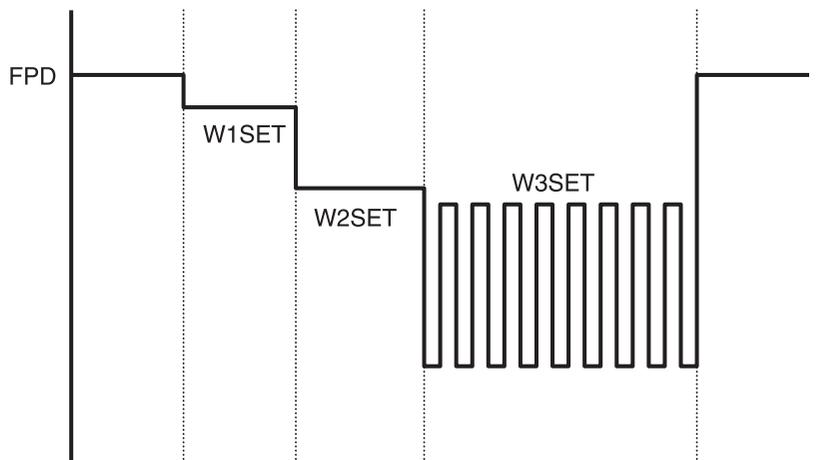
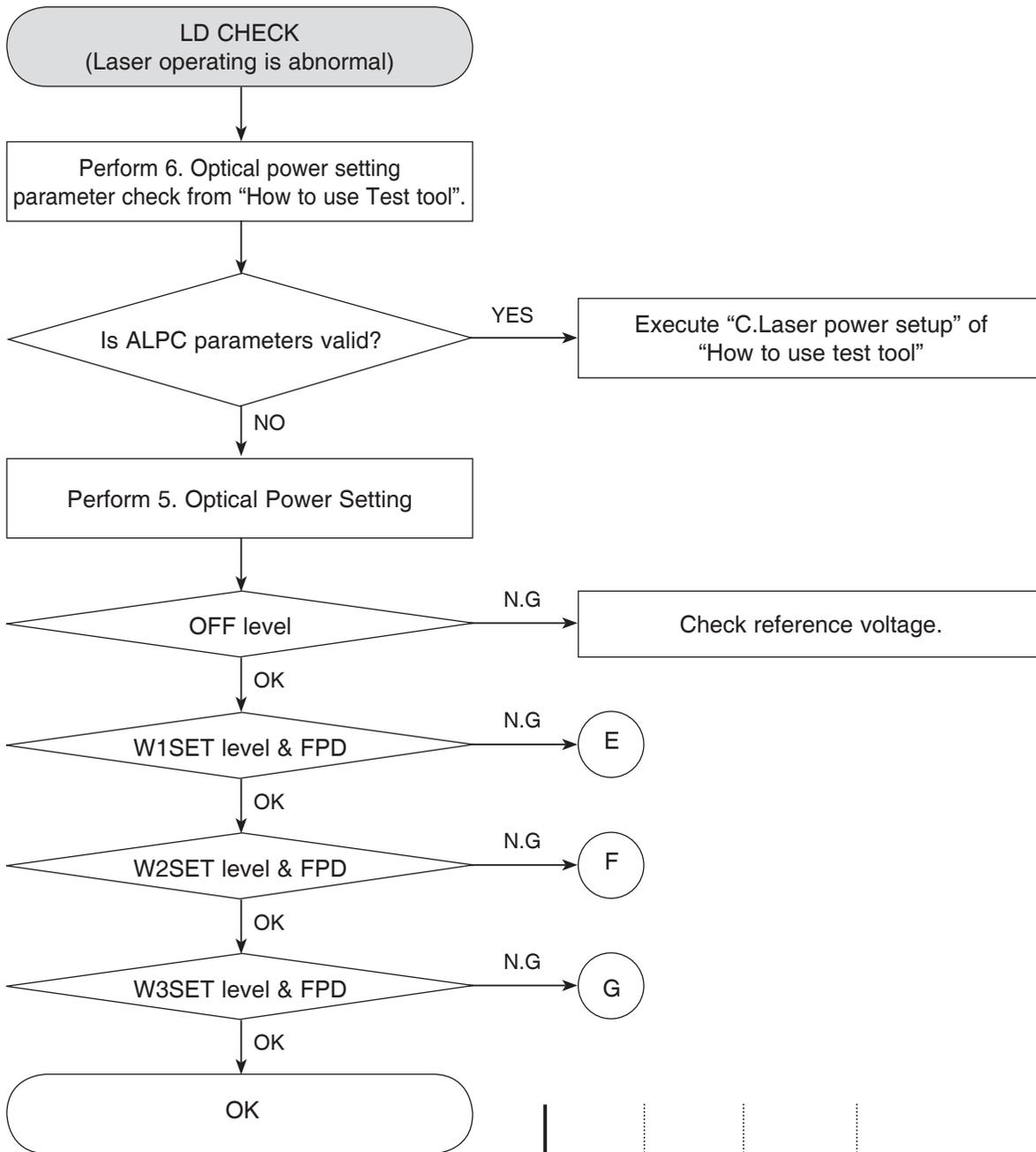
* LIC101 pin20 is MOUT1(FEP Monitor1). After disc recognition action, Monitor port is off. So, please check TE signal during disc recognition.

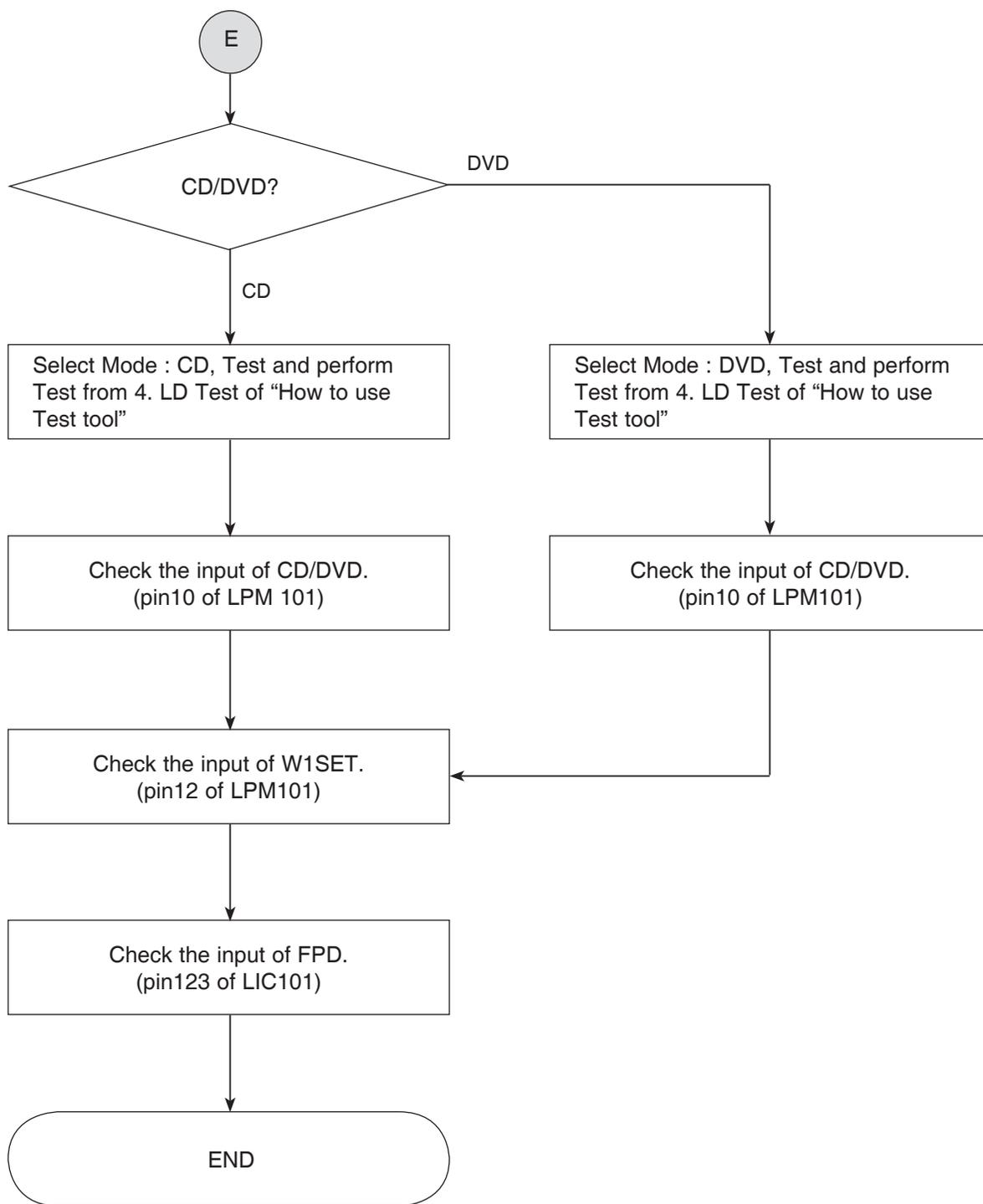


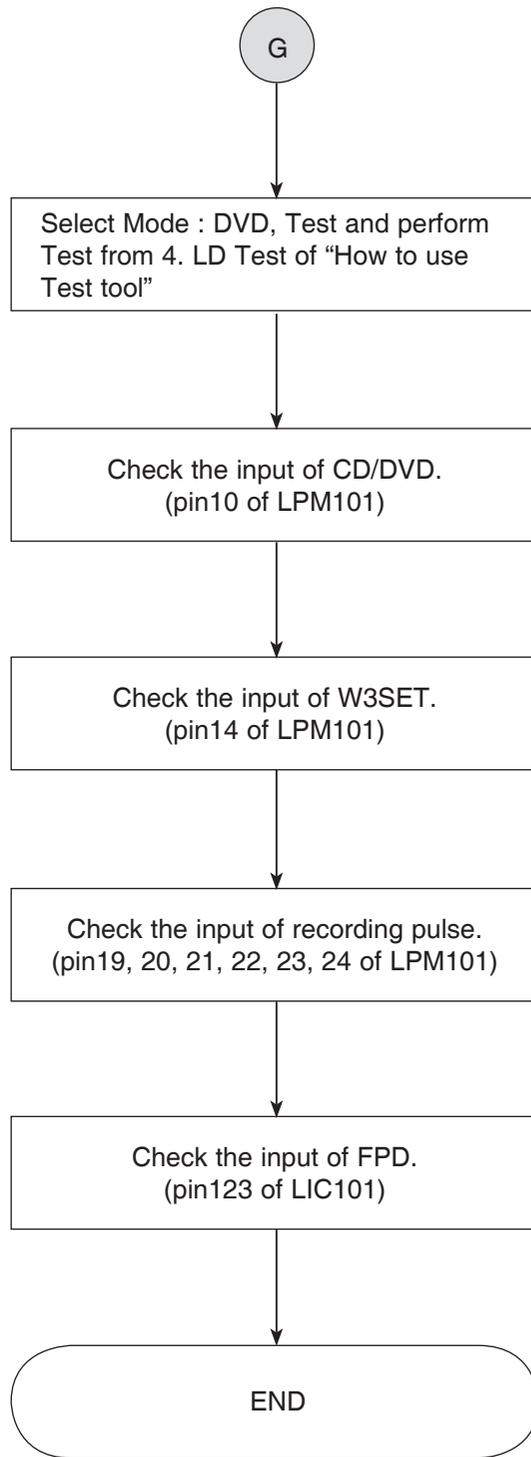
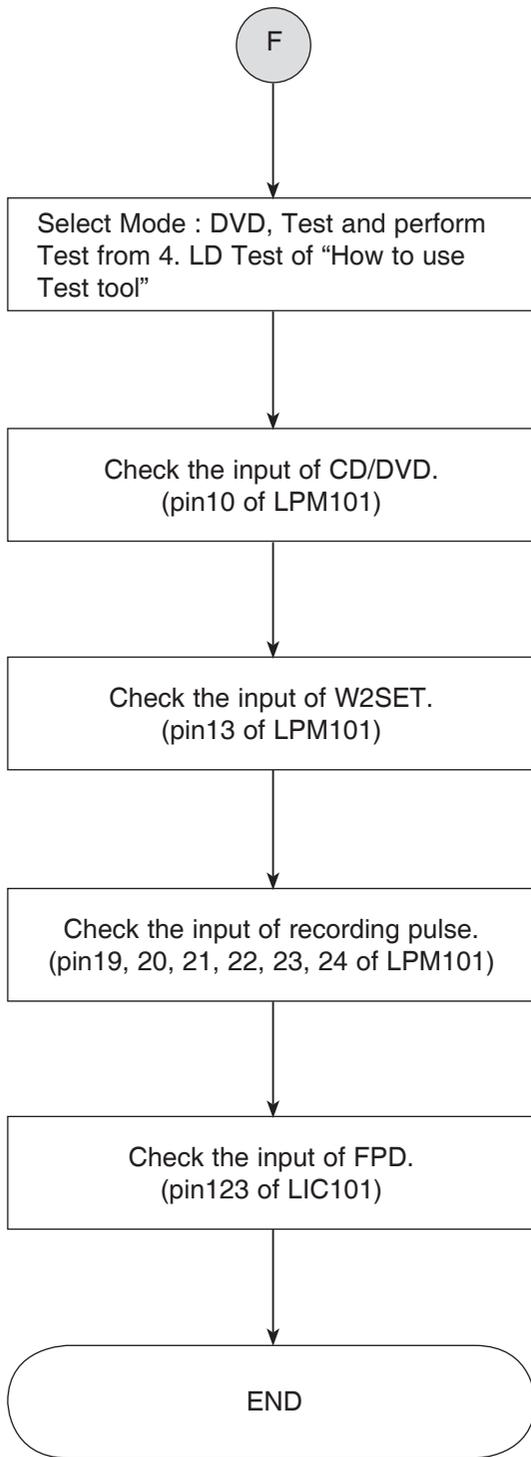








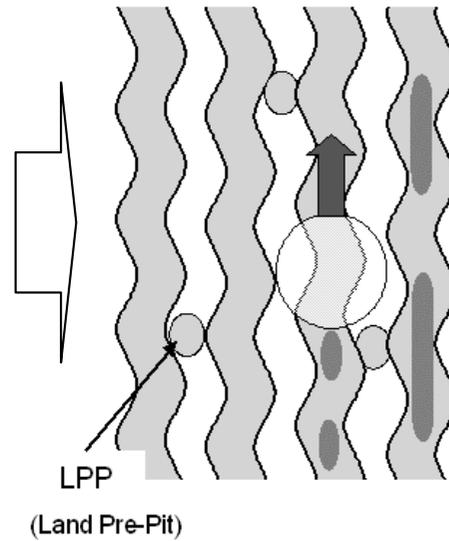
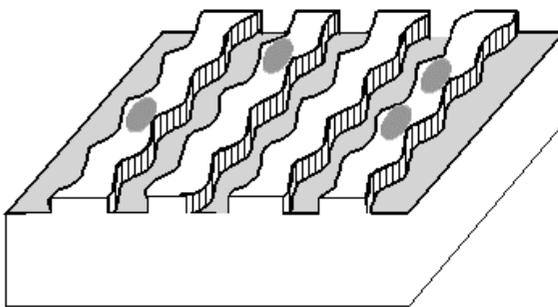
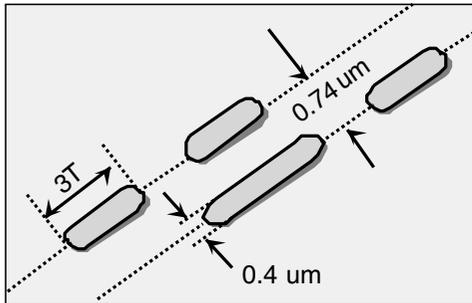




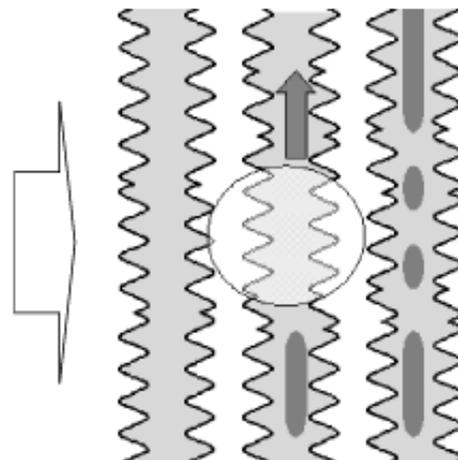
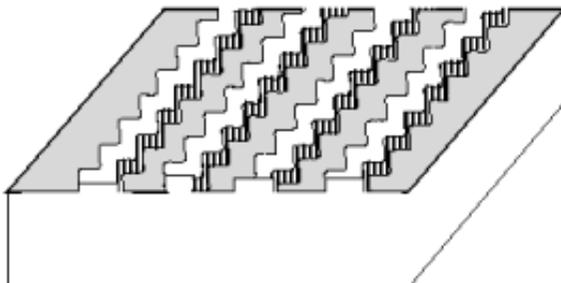
THE DIFFERENCE OF DVD-R/RW, DVD+R/RW DISCS AND DVD-ROM

1. RECORDING LAYER

- DVD-ROM (Read Only Disc)



- DVD+R/RW Disc

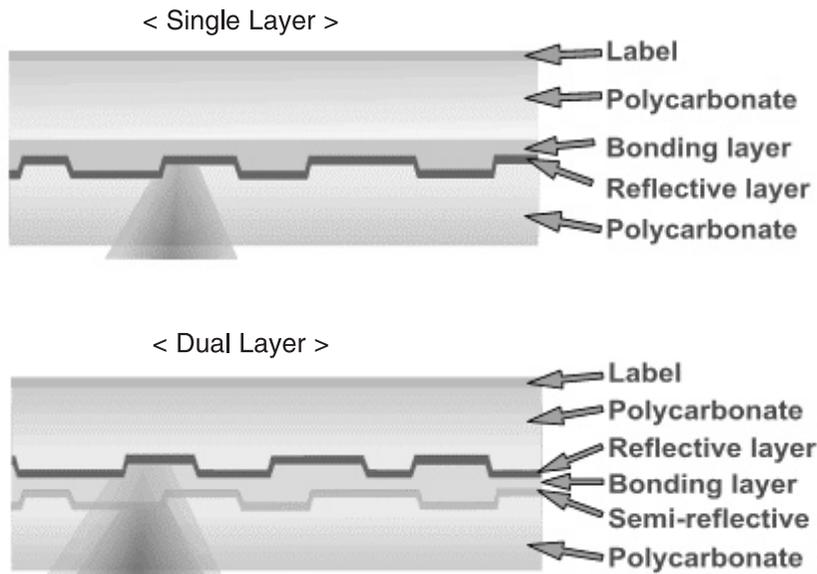


2. DISC SPECIFICATION

	DVD-ROM		DVD-R	DVD-RW	DVD+R	DVD+RW
	Single-Layer	Dual-Layer				
Media Type	Read Only	Read Only	Dye	Phase change	Dye	Phase change
User data capacity	4.7GB	8.54GB	4.7GB	4.7GB	4.7GB	4.7GB
Wavelength	650nm	650nm	650nm	650nm	650nm	650nm
Reflectivity	45~85%	18~30nm	45~85%	18~30%	45~85%	18~30nm
Track pitch	0.74 μ m	0.74 μ m				
Minimum pit length	0.4 μ m	0.4 μ m				
Modulation	>0.6	>0.6	>0.6	>0.6	>0.6	>0.6
Channel bit-rate	26.16MHz	26.16MHz	26.16MHz	26.16MHz	26.16MHz	26.16MHz
Wobble Frequency	–	–	140KHz	140KHz	817.4KHz	817.4KHz
Addressing	26.16MHz	26.16MHz	Wobble & LPP	Wobble & LPP	Wobble(ADIP)	Wobble(ADIP)
Read Power (mW)					0.7 \pm 0.1	0.7 \pm 0.1
Write Power (mW)	–					
Jitter	<8%	<8%	<8%	<8%	<9%	<9%

3. DISC MATERIALS

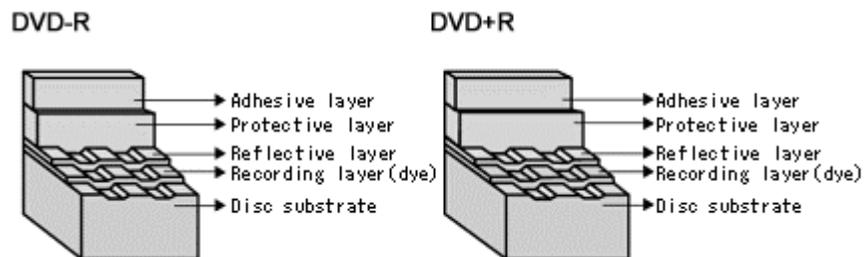
1) DVD-ROM



2) Recording format using organic dye material (DVD-R / DVD+R)

The format that records data through the creation of recorded marks by changing the organic dye material with a laser beam.

• Disc structure



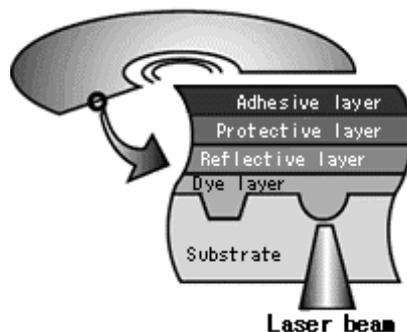
• Recording principles

[Recording]

Recording is done by changing the organic dye layer and the substrate with a laser. When a strong laser is applied to a disc, the temperature of the organic dye material goes up, the dye is decomposed and the substrate changes at the same time. At this time, a durable bit is created as is the case with a CD-ROM.

[Playback]

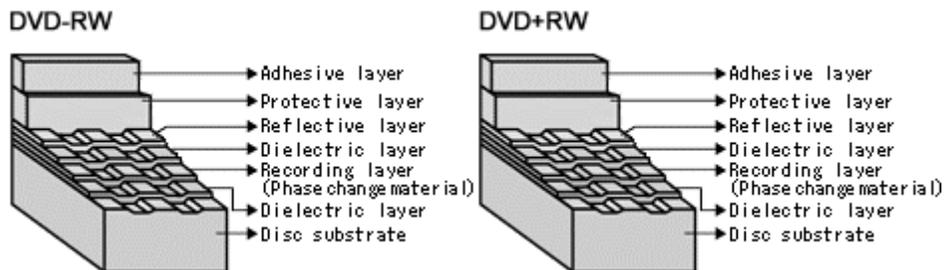
Signals are read with the differences of the reflection of a laser from pits.



3) Recording format using phase-change recording material (DVD-RW / DVD+RW)

Data is recorded by changing the recording layer from the amorphous status to the crystalline status, and played back by reading the difference of the reflection coefficient.
Amorphous: Non-crystalline.

• Disc structure



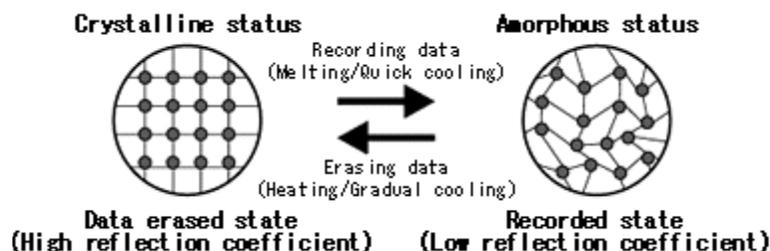
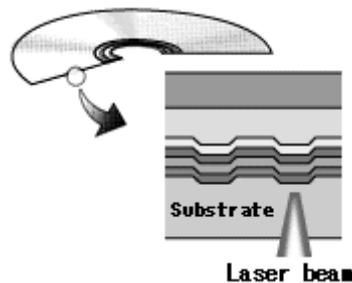
• Recording principles

[Recording]

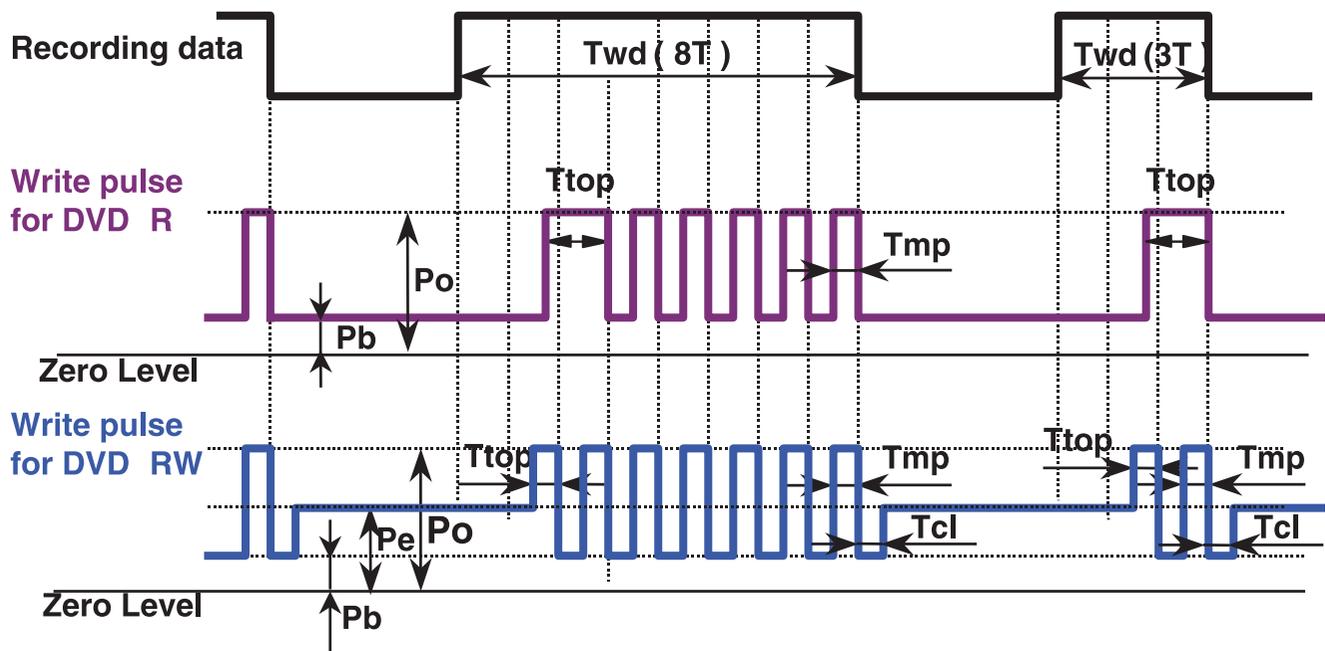
When a high-power laser is applied to the recording material, it melts and then becomes amorphous with a low reflection coefficient when it quickly cools off. When a mid-power laser is applied to heat gradually the recording material and then gradually cools it off, it becomes crystal with a high reflection coefficient.

[Playback]

A low-power laser is used for playback. The amount of reflected light depends on the status (amorphous or crystalline) of the recording material. This is detected by an optical sensor.



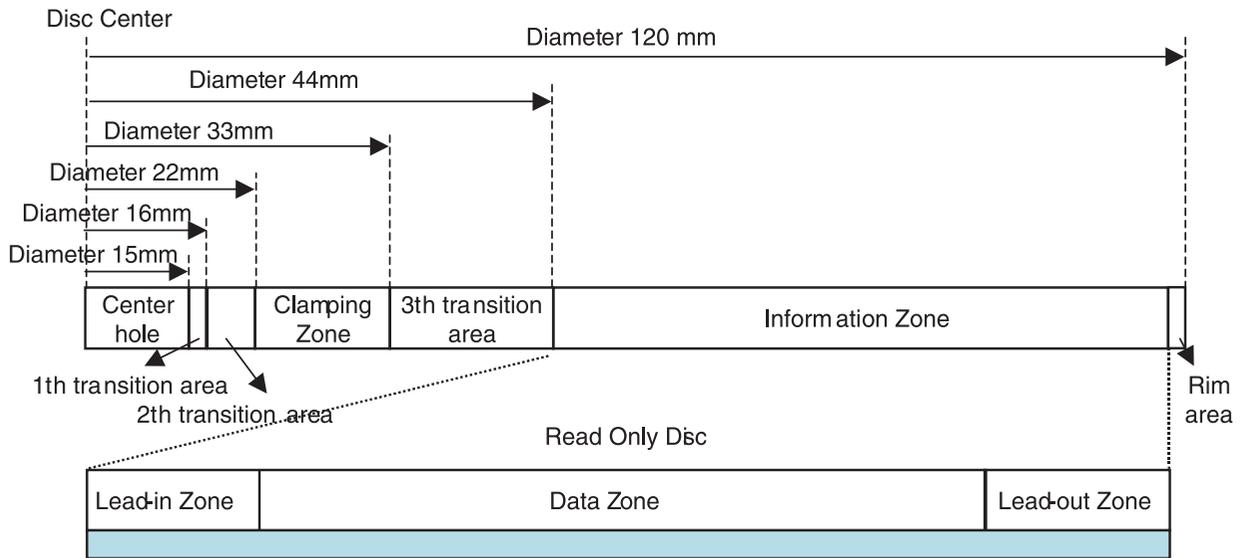
To make recordings, it is necessary to modulate the write pulse, which is called "Write Strategy". There can be many types in Write Strategy. Typically Write Strategy for DVD \pm R has NMP(Non Multi-Pulse) type and MP(Multi-Pulse) type. In NMP type each single mark is created by subsequent separated short pulses. In MP type each single mark is created by one continuous pulse. Write Strategy for DVD \pm RW has Type 1 and Type 2. In Type 1 the mark with nT width is created by one top pulse and $(n-2)$ multi-pulses. Thus mark $3T$ is made by one top pulse and one multi-pulse. In Type 2 the mark with nT width is created by one top pulse and $(n-3)$ multi-pulses. Thus mark $3T$ is made by one top pulse only. RS-06A uses MP type Write Strategy for DVD \pm R and Type 1 for DVD \pm RW as shown below.



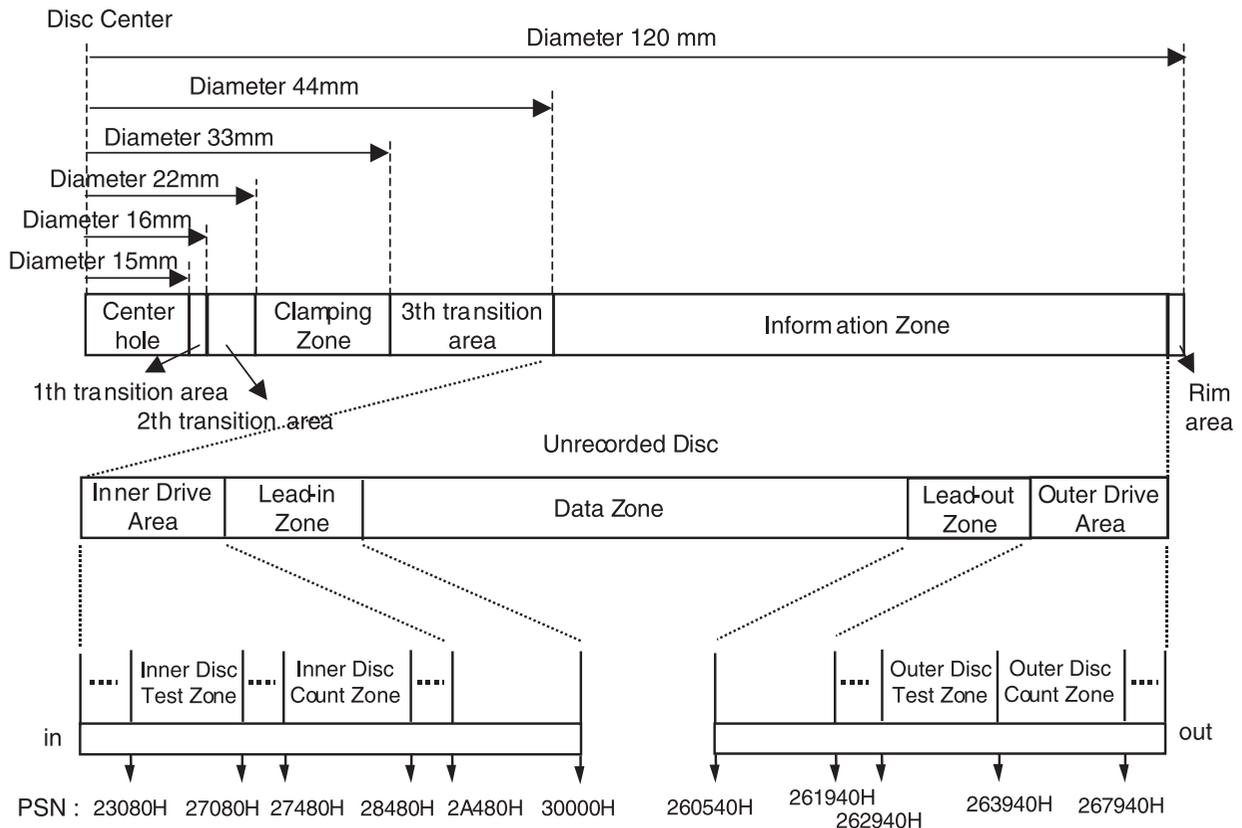
P_o :Write Power (Peak Power)
 P_e :Erase Power
 P_b :Bias Power

4. ORGANIZATION OF THE INNER DRIVE AREA, OUTER DRIVE AREA, LEAD-IN ZONE AND LEAD-OUT ZONE

1) Layout of DVD-ROM disc

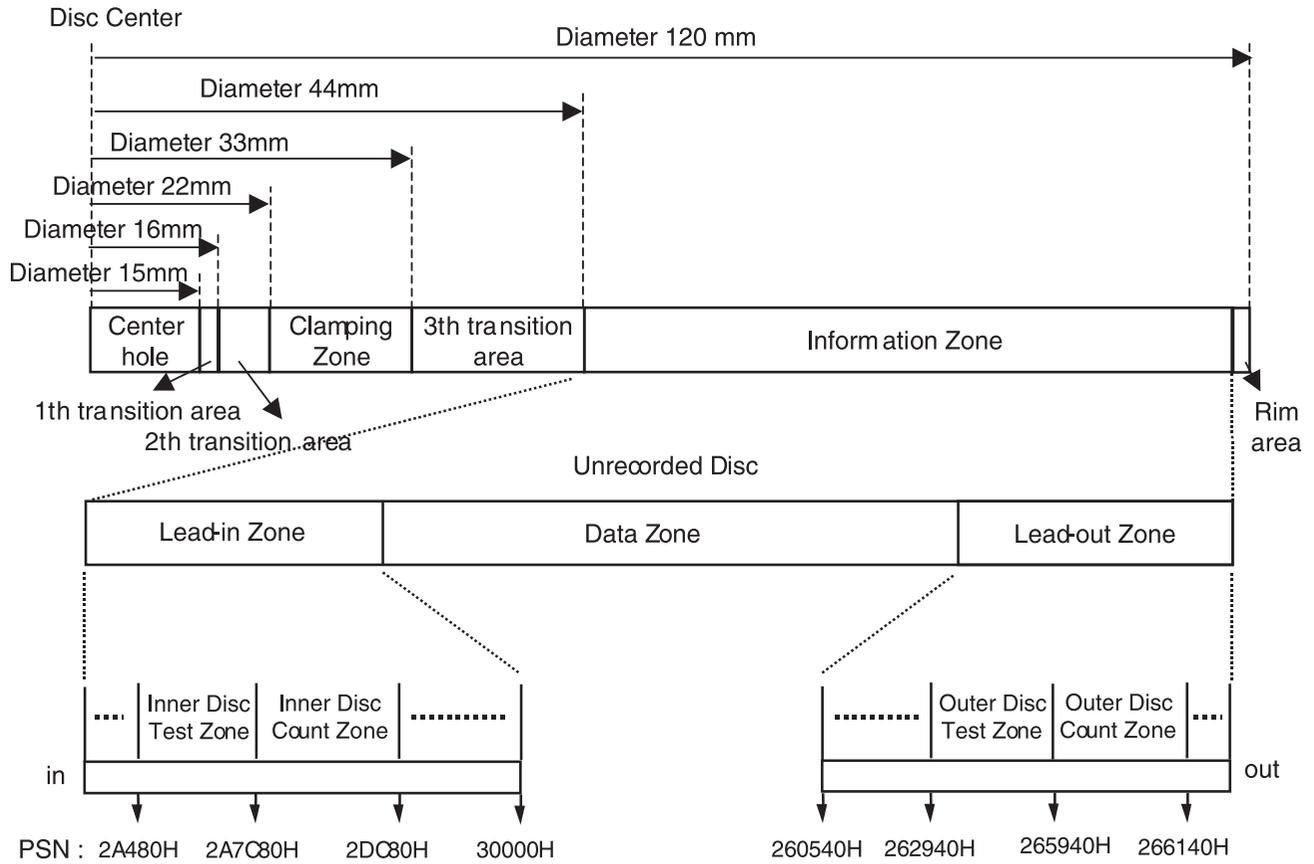


2) Layout of DVD+R disc



Inner Disc Test Zone : for performing OPC procedures.
 Inner Disc Count Zone : For counting the number of OPC algorithm performed in IDT Zone.
 Outer Disc Test Zone : for performing OPC procedures.
 Outer Disc Count Zone : For counting the number of OPC algorithm performed in IDT Zone.

3) Layout of DVD+RW disc



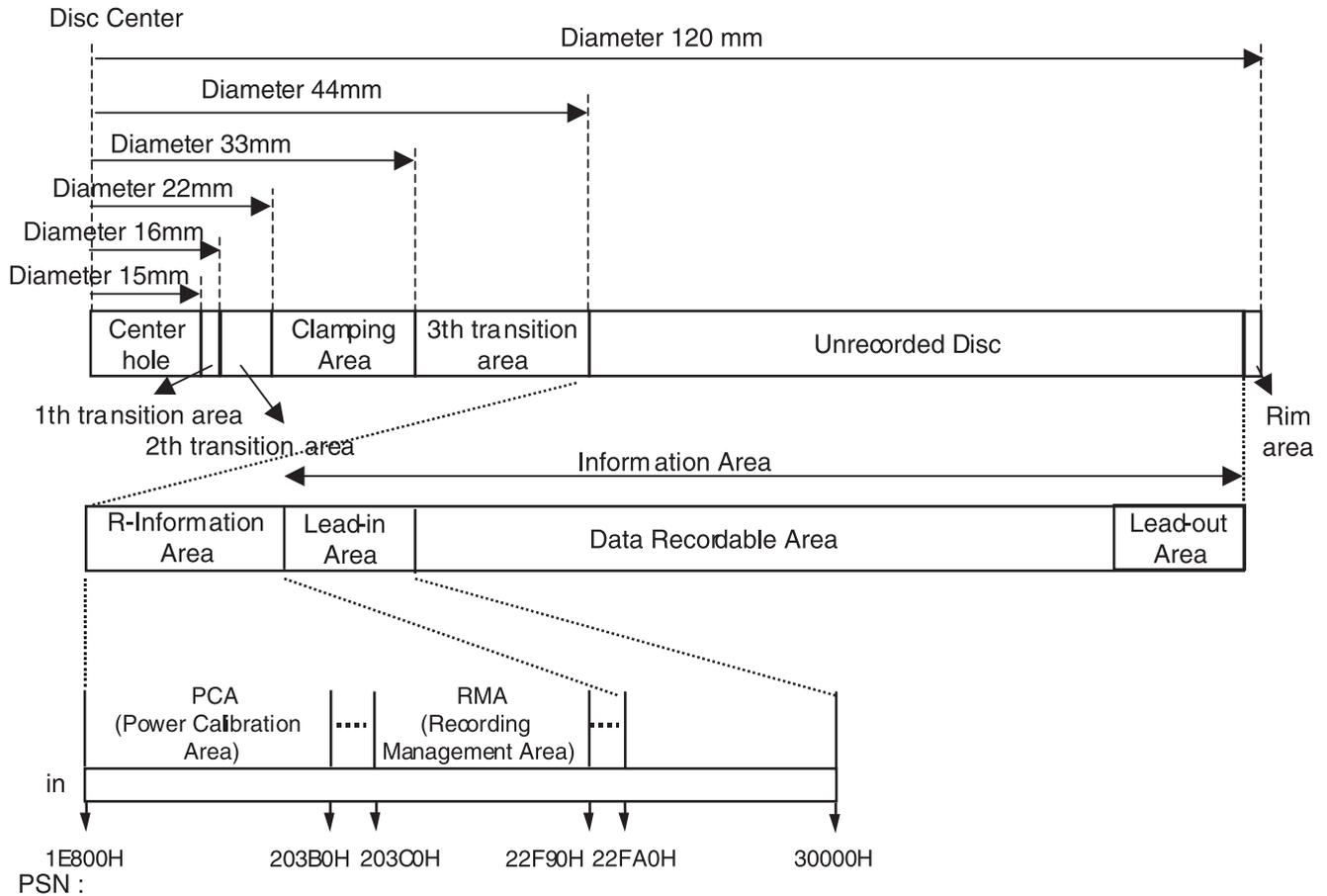
Inner Disc Test Zone : for performing OPC procedures.

Inner Disc Count Zone : For counting the number of OPC algorithm performed in IDT Zone.

Outer Disc Test Zone : for performing OPC procedures.

Outer Disc Count Zone : For counting the number of OPC algorithm performed in IDT Zone.

4) Layout of DVD-R/RW disc



OPTICAL POWER SETTING

1. MANUAL OPTICAL POWER SETTING

If the manual optical power setting is not accomplished, you can use the automatic optical power setting on page 4-30.

1-1. ALPC Measurement System

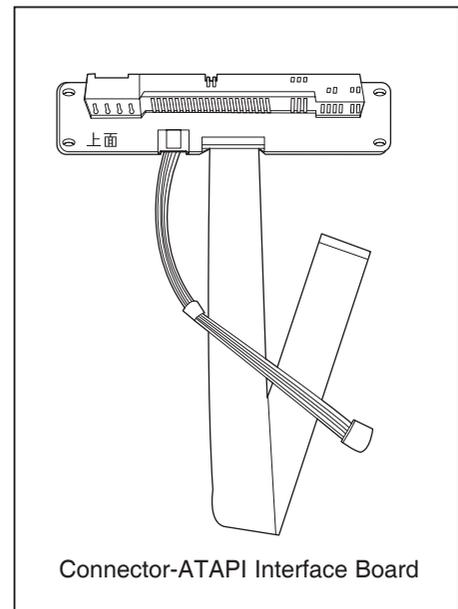
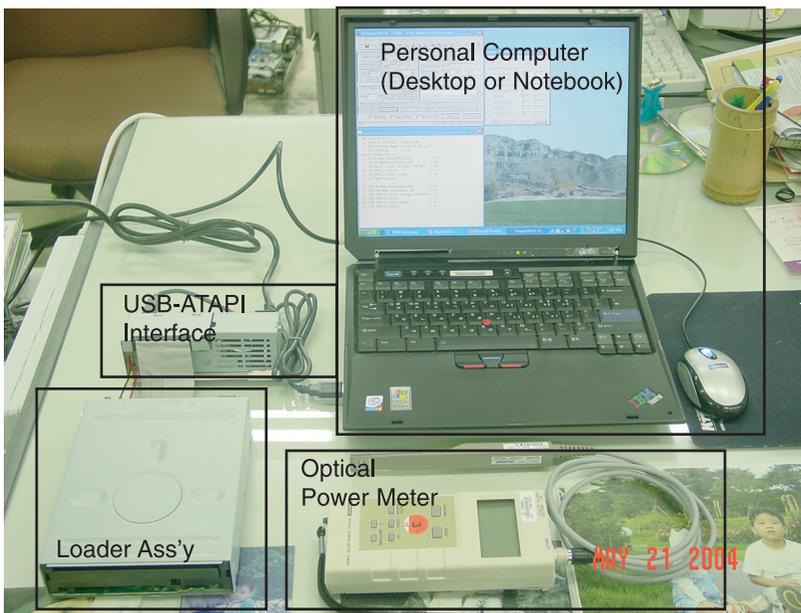
We need basically several measurement instruments to adjust Optical Power of CD and DVD Disc

- **ESSENTIAL INSTRUMENT**

- 1) Optical Power meter & Sensor (ADVANTEST, TQ8230/Q82014A)
- 2) Personal Computer
- 3) Adjustment Program (Dragon or ALPC) --> being recommended ALPC Program in case of SVC

- **OPTIONAL INSTRUMENT**

- 1) USB-ATAPI Interface (if you don't have Notebook which has ATAPI Interface or use PC USB Port)
- 2) Connector-ATAPI Interface Board



1-2. ALPC Program

Use the ALPC program in Dragon tool for Optical power setting. It is consist of total 4 files.

Dragon_JW3P.exe
dragon.cfg
blue.dat
WNASPI32.DLL

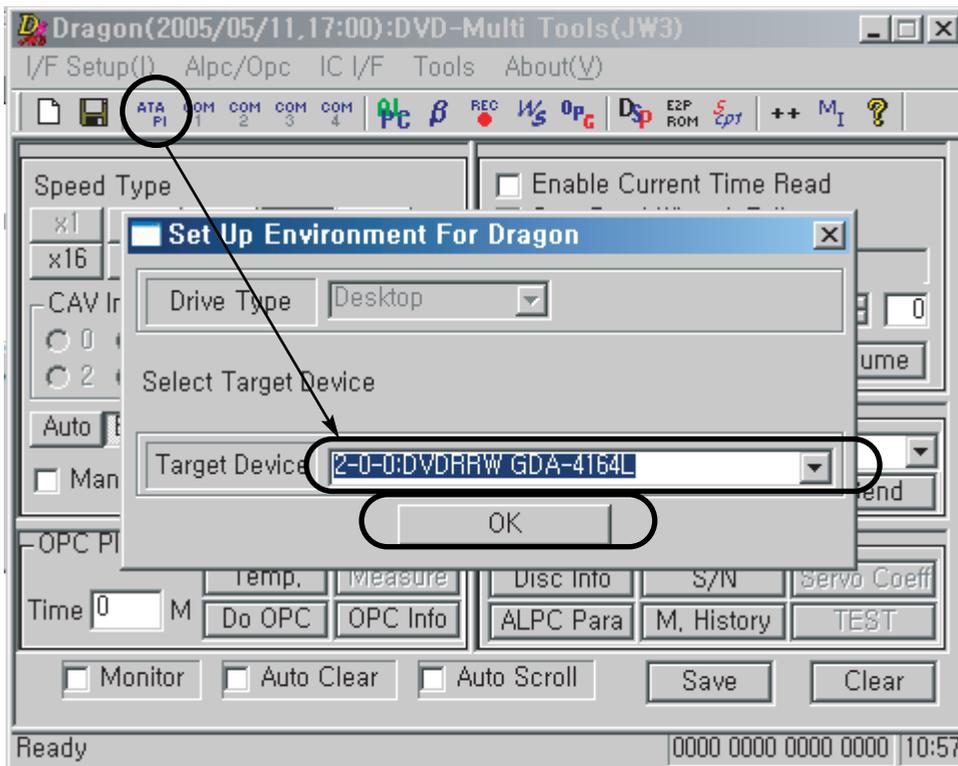
Four files must exist in same Directory.

1-3. Execute ALPC Program

1) Execute Dragon_JW3P.exe file.

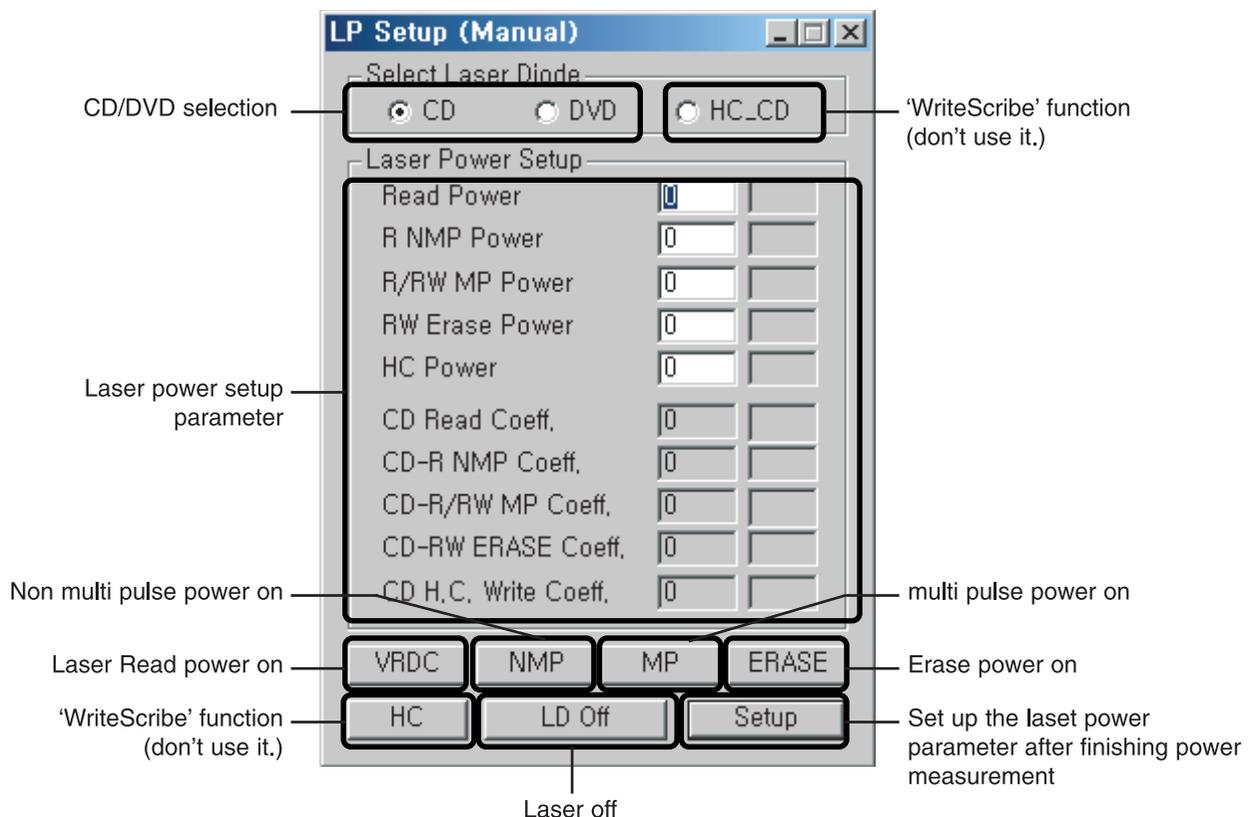
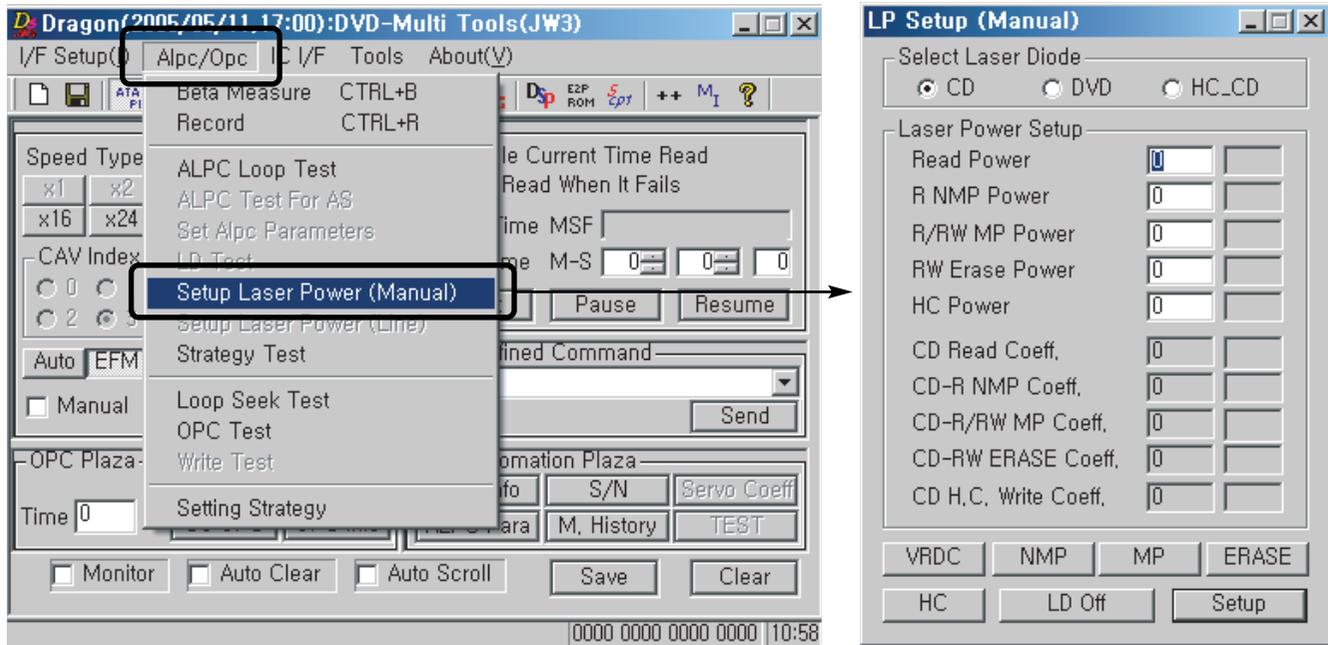


2) Enter the password. It is "qaz".
When you enter the password, turn off the "Caps lock" in your keyboard.



3) Set up the target device.
Press "ATAPI" button on the main dialog of Dragon tool. And find the target device which is GDA-4164L.

- 4) If the target device setting is completed, execute the “Setup Laser Power(Manual)” in the “Alpc/Opc” menu.



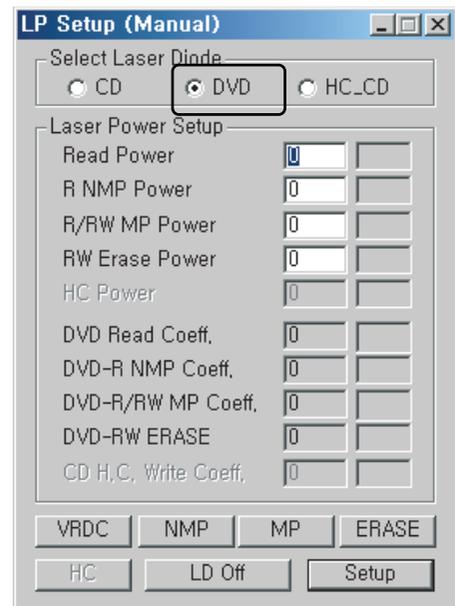
1-4. Optical power setting

<Test for checking DVD LD and CD LD>

When you change the Travers ass'y(including pick-up) or loader PCB, you must do the laser power setting to match pick-up and loader PCB.

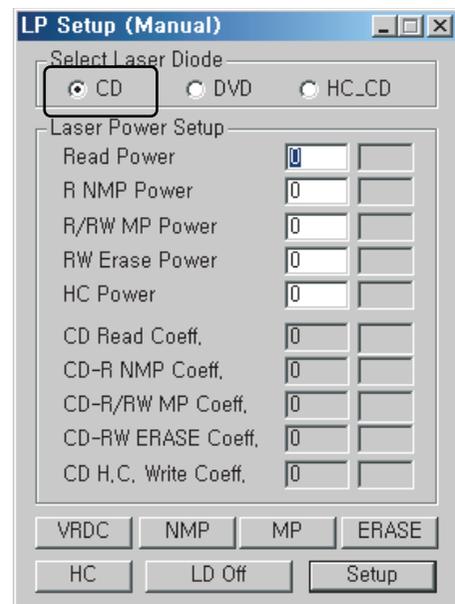
1) DVD LD power setting

- Select the DVD in the “Select Laser Diode”
- Press **VRDC** (Read power on, Strong read light)
- Measure optical read Power.
- Write read power value.
- In case of **NMP** **MP** **ERASE** ,
you are able to measure the power through same procedure.
(caution) Don't watch light directly.
- When you finish optical power measurement,
press **LD Off** button(LD Off).
- Press **Setup** button.(save to ERPROM)



2) CD LD Power Setting

- Select the CD in the “Select Laser Diode”
 - Press **VRDC** .
 - Measure optical read Power.
 - Write Read Power value.
 - Press **Setup** button(save to ERPROM)
- *** In case of CD power setting of RS-06A, loader doesn't need to set up write power.
Although NMP, MP, Erase and HC power is N.G when you press setup, please ignore the N.G message.
Because of RS-06A only support reading function about CD-R/RW.
- * Look at reference sheet to test Optical Power.
** Power value is mW unit. Value is read power X 100.



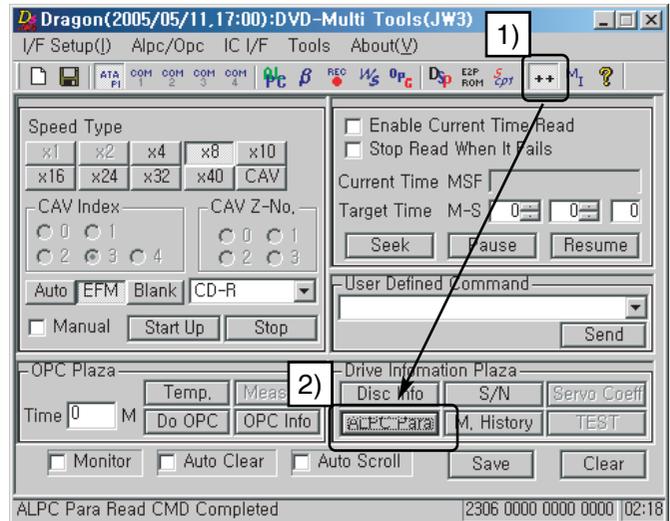
1-5. Confirm Optical Power Setting Parameter

LD Test result is ok, but Loader performance is bad.

1. Check ALPC parameter value

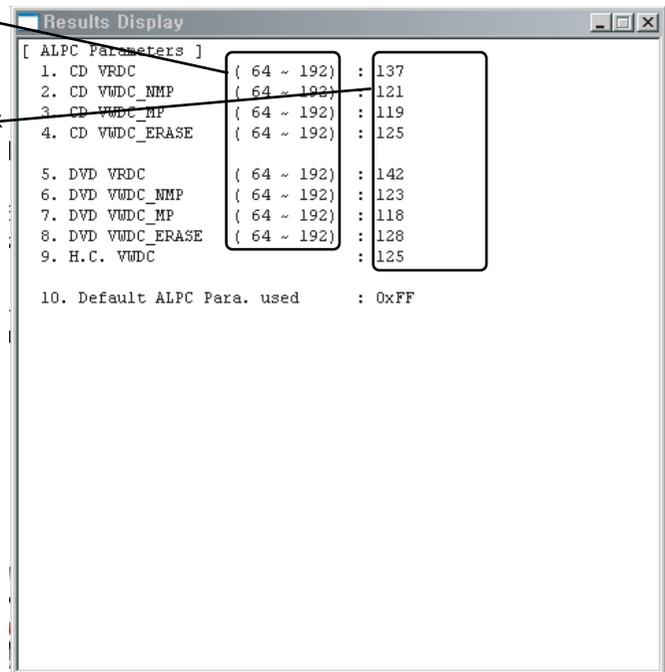
- 1) Press **++** button to open "Results Display" dialog.
- 2) Press **ALPC Para** button.

- We can see optical power setting value.
- Write optical Power Setting value to paper.
- Adjust power setting again.
- Compare original parameter to new parameter.
- if parameter value is different, original value is wrong or optical power may change.
- But pick-up LD test is all ok, just adjust optical power setting again.



Normal range of ALPC parameter

Optical power value which has been saved in the EEPROM

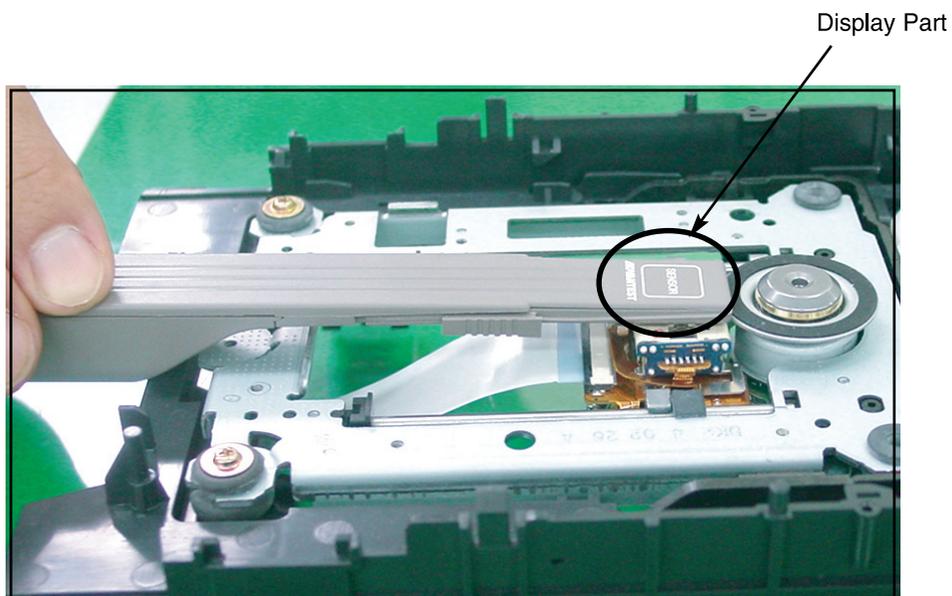


1-6. Attachment. Optical Power Measurement

Optical Power measurement is to adjust LD power from Pick-up
To measure optical power, LD status is on. Other light affects optical power.
Avoid other light to measure exact power
Generally headlight power is about 50 μ W, Sun power is about 100mW.

Optical Power measurement method

1. Fit optical Power Meter λ (wavelength) value to DVD.(generally 660nm)
2. DVD LD On.
3. Approach power sensor to Pick-up Lens about 3mm vertically. Fix Lens and Sensor mark position.
4. Read Monitor value. (move sensor read just a little and read max value.)
(caution) unit is mW.
5. Write monitoring value x 100. Only an integer.
6. Fit Power Meter (wavelength) value to CD.(generally 780nm)
7. CD LD On.
8. 3 ~ 5 recheck.



2. AUTOMATIC OPTICAL POWER SETTING (SET-BASED)

The RS-06A mounted models are supported by the B/END to automatically execute the optical power setting of the loader at the set condition with the following steps.

1. Use the remote controller to select the mode as Lock position at the Setup menu.
2. Use the remote controller to enter 5 -> 7 -> 2 -> 0 into the set.
When they are normally entered, the GUI is displayed as shown at Fig. 1.
3. When you select 'Yes', the optical power setting is automatically proceeded and it takes about 20 seconds.
4. When setting is finished, OK or NG is displayed on the screen.
The OK screen is displayed for the normal termination (Fig. 2)
The NG screen is displayed for the abnormal termination (Fig. 3)
5. When you select 'Yes' button, the GUI is cleared and it normally operates.



Fig. 1



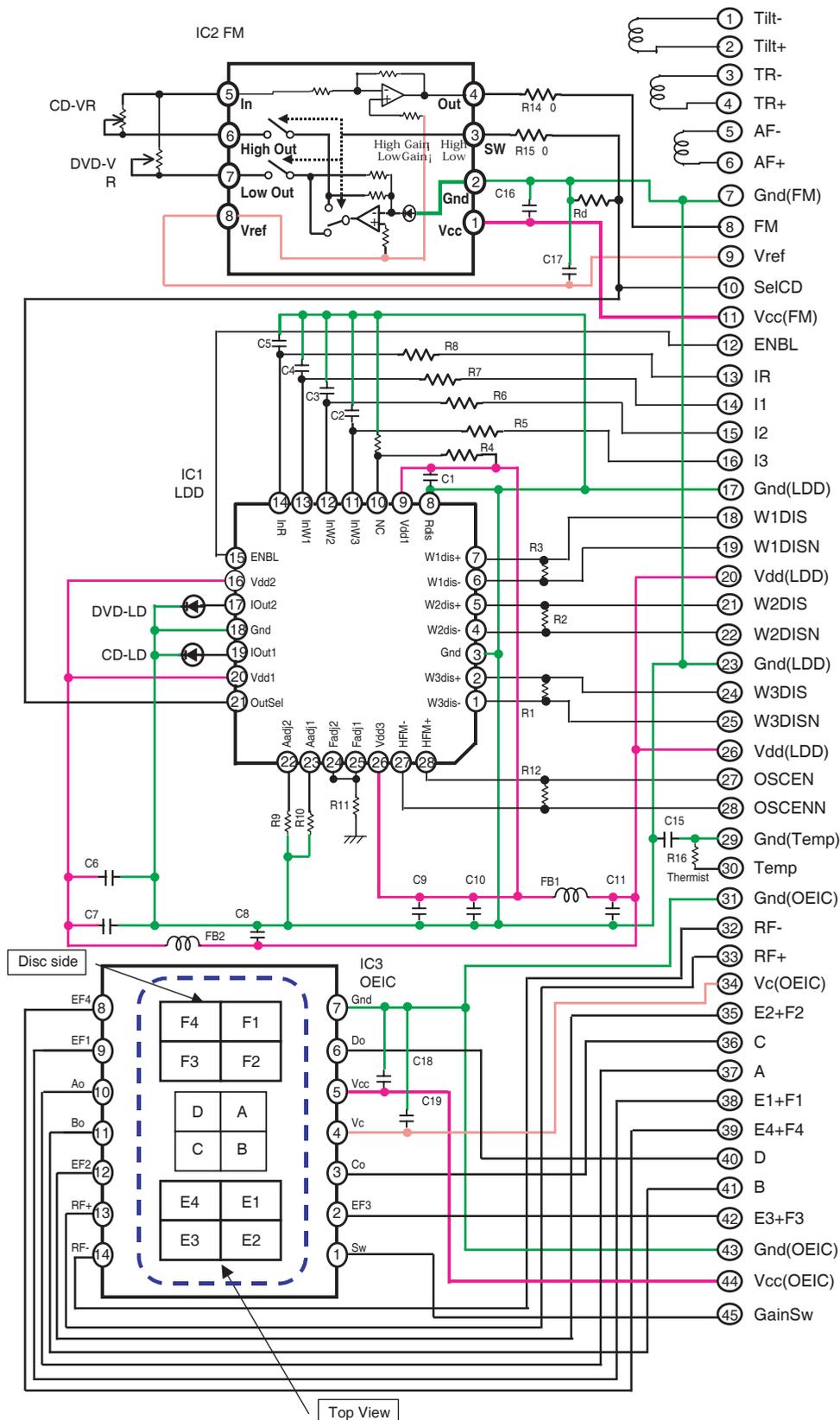
Fig. 2



Fig. 3

INTERNAL STRUCTURE OF THE PICK-UP

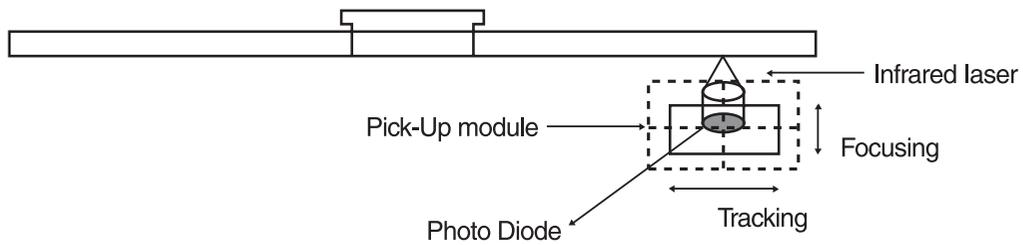
1. BLOCK DIAGRAM OF THE PICK-UP (HOP-7232TL)



2. PICK UP PIN ASSIGNMENT

No.	Signal Name	Signal Description	I/O
1	Tilt-	Tilting Actuator drive signal -	I
2	Tilt+	Tilting Actuator drive signal +	I
3	TR-	Tracking Actuator drive signal -	I
4	TR+	Tracking Actuator drive signal +	I
5	AF-	Focusing Actuator drive signal -	I
6	AF+	Focusing Actuator drive signal +	I
7	Gnd(FM)	Ground connection for FM	
8	FM	FM output	O
9	Vref	FM reference voltage input	I
10	SELCD	High:selects CD-LD,CD-VR Low: selects DVD-LD,DVD-VR	I
11	Vcc(FM)	Power supply for FM (+5 V)	
12	ENABLE	Disables output current regardless of **DIS (Low voltage:No lout)	I
13	IR	Input current for current amplifier	I
14	I1	Input current for current amplifier	I
15	I2	Input current for current amplifier	I
16	I3	Input current for current amplifier	I
17	GND(LDD)	Ground connection for LDD	
18	W1DIS	LVDS control for output current (Low active) (LVDS+)	I
19	W1DISN	LVDS control for output current (LVDS-)	I
20	VDD(LDD)	Power supply for LDD (+5 V)	
21	W2DIS	LVDS control for output current (Low active) (LVDS+)	I
22	W2DISN	LVDS control for output current (LVDS-)	I
23	Gnd(LDD)	Ground connection for LDD	
24	W3DIS	LVDS control for output current (Low active) (LVDS+)	I
25	W3DISN	LVDS control for output current (LVDS-)	I
26	Vdd(LDD)	Power supply for •DD (+5 V)	
27	OscEn	LVDS control for Oscillator (High active) (LVDS+)	I
28	OscEnN	LVDS control for Oscillator (LVDS-)	I
29	Gnd(TEMP)	Ground connection for Thermister	
30	TEMP	Resistance for controlling temperature	O
31	Gnd(OEIC)	Ground for OEIC	O
32	RF-	Signal OEIC RF negative differential output	O
33	RF+	Signal OEIC RF positive differential output	O
34	Vc(OEIC)	Reference voltage input for OEIC (+2.1 V)	I
35	E2+F2	Signal OEIC output EF2	O
36	C	Signal OEIC output C	O
37	A	Signal OEIC output A	O
38	E1+F1	Signal OEIC output EF1	O
39	E4+F4	Signal OEIC output EF4	O
40	D	Signal OEIC output D	O
41	B	Signal OEIC output B	O
42	E3+F3	Signal OEIC output EF3	O
43	Gnd(OEIC)	Ground for OEIC	
44	Vcc(OEIC)	Power supply for OEIC (+5 V)	I
45	GainSw	OEIC output gain control (High voltage:Low gain , Middle:Middle gain , Low:High gain)	I

3. SIGNAL DETECTION OF THE P/U



1) Focus Error Signal ==> $(A+C)-(B+D)$

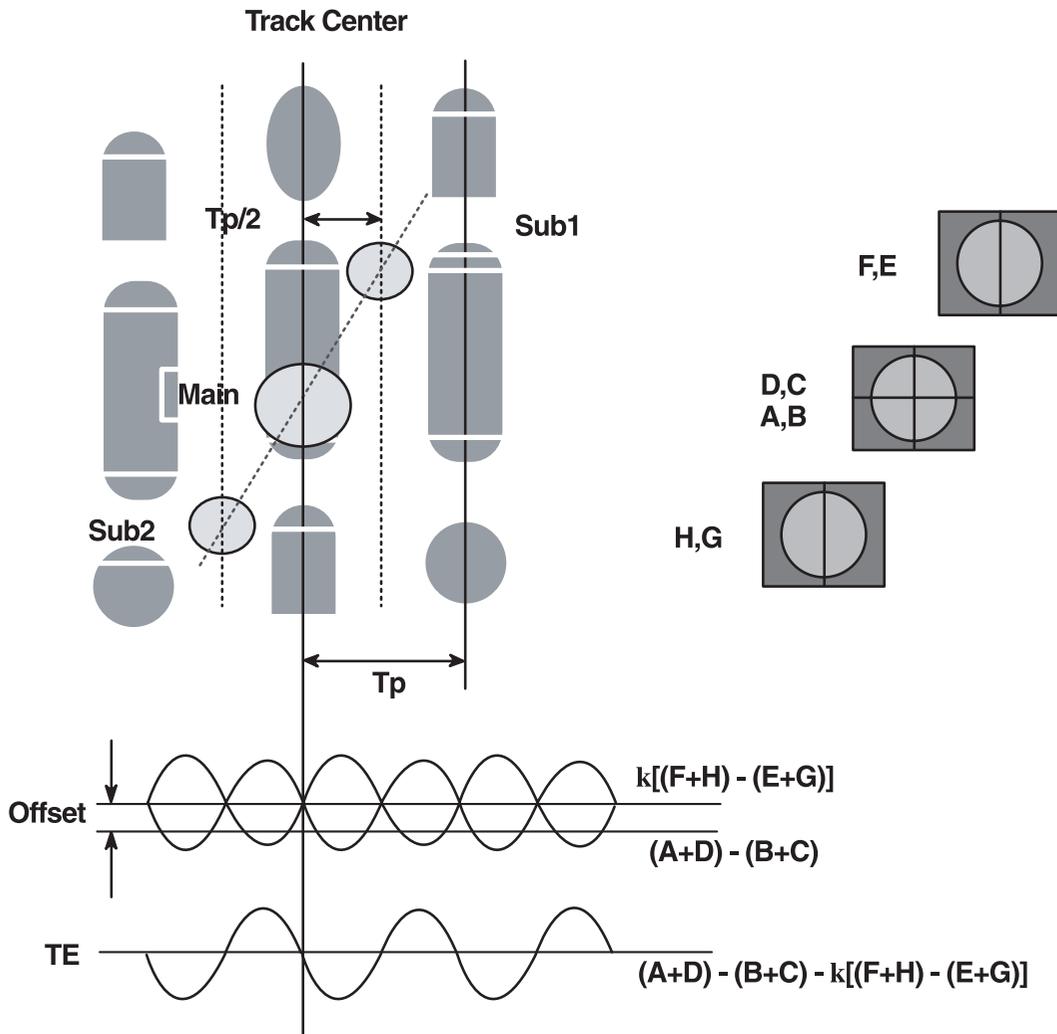
This signal is generated in RF IC (LIC121 : AN22113A) and controls the pick-up's up and down to focus on Disc.

2) Tracking Error Signal (DPP Method) ==> $\{(A+D)-(B+C)\} - k \times \{(EF1+EF4)-(EF2+EF3)\}$

This signal is generated in RF IC (LIC121 : AN22113A) and controls the pick-up's left and right shift to find track on Disc.

3) RF Signal ==> $(A+B+C+D)$

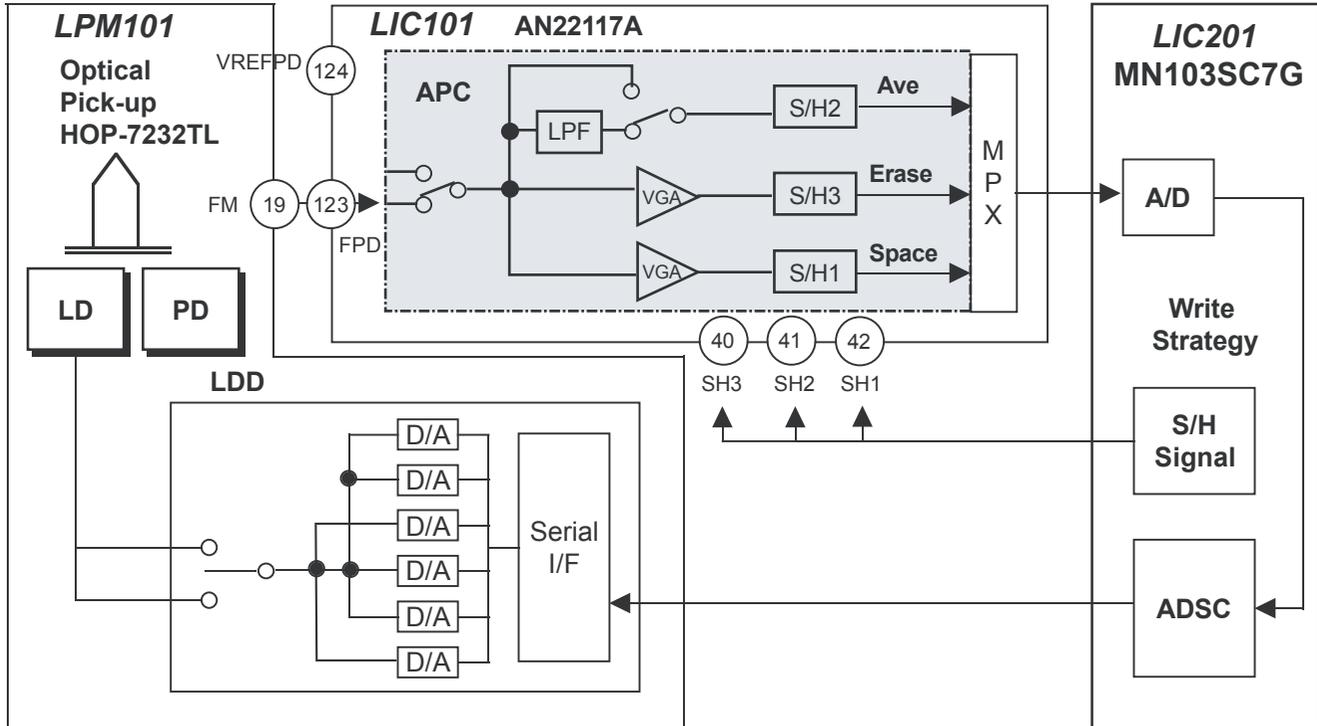
This signal is converted to DATA signal in DSP IC (LIC201 : MN103SA6G).



DESCRIPTION OF CIRCUIT

1. ALPC (AUTOMATIC LASER POWER CONTROL) CIRCUIT

1-1. Block Diagram

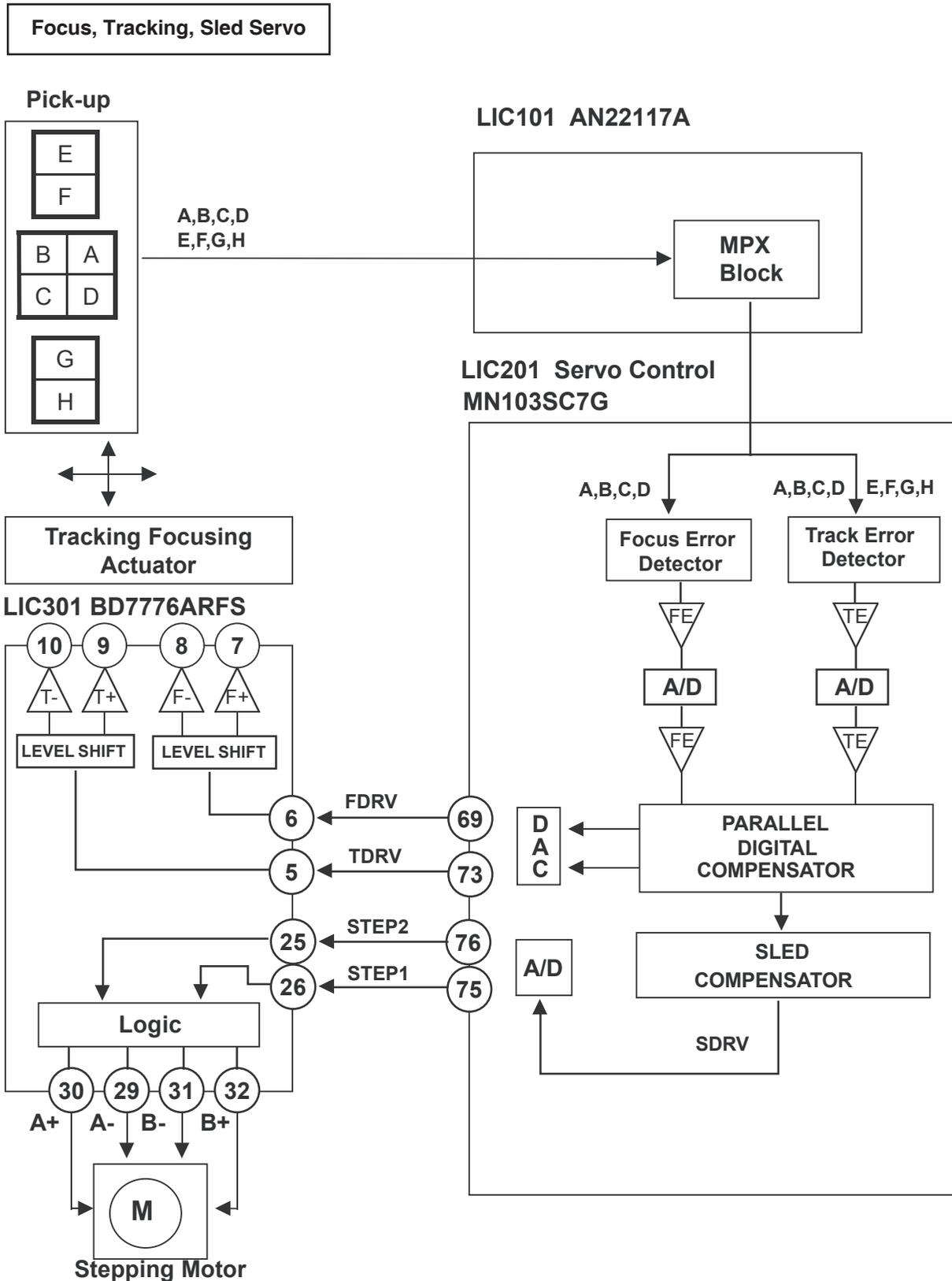


1-2. ALPC (Automatic Laser Power Control) Circuit Operation

The ALPC block detects the laser output power of the front monitor. The power signal detected with the PD for front monitor detection is input the voltage from the VPD pin(123Pin), the reference signal of the input signal is input from the VREFPD pin(124Pin). The ALPC block generates the singals from the input laser power signals in the following detection systems. This block has four detection paths:All average value path, multi pulse average/peak value detection path, erase/bottom value detection path, space/playback power value detection path.

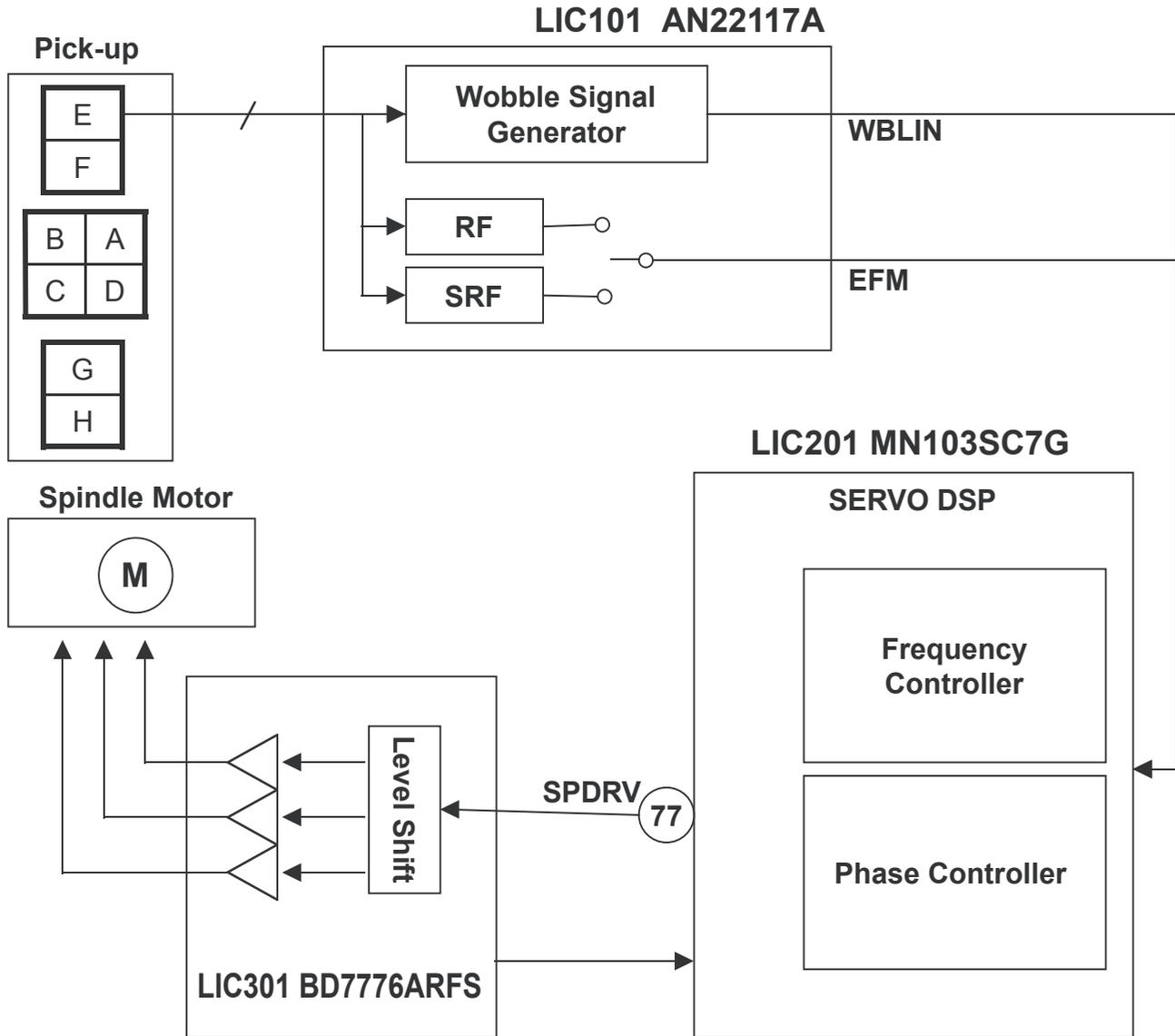
2. FOCUS/TRACKING/SLED SERVO CIRCUIT

2-1. Focus, Tracking & Sled Servo Process



3. SPINDLE SERVO CIRCUIT

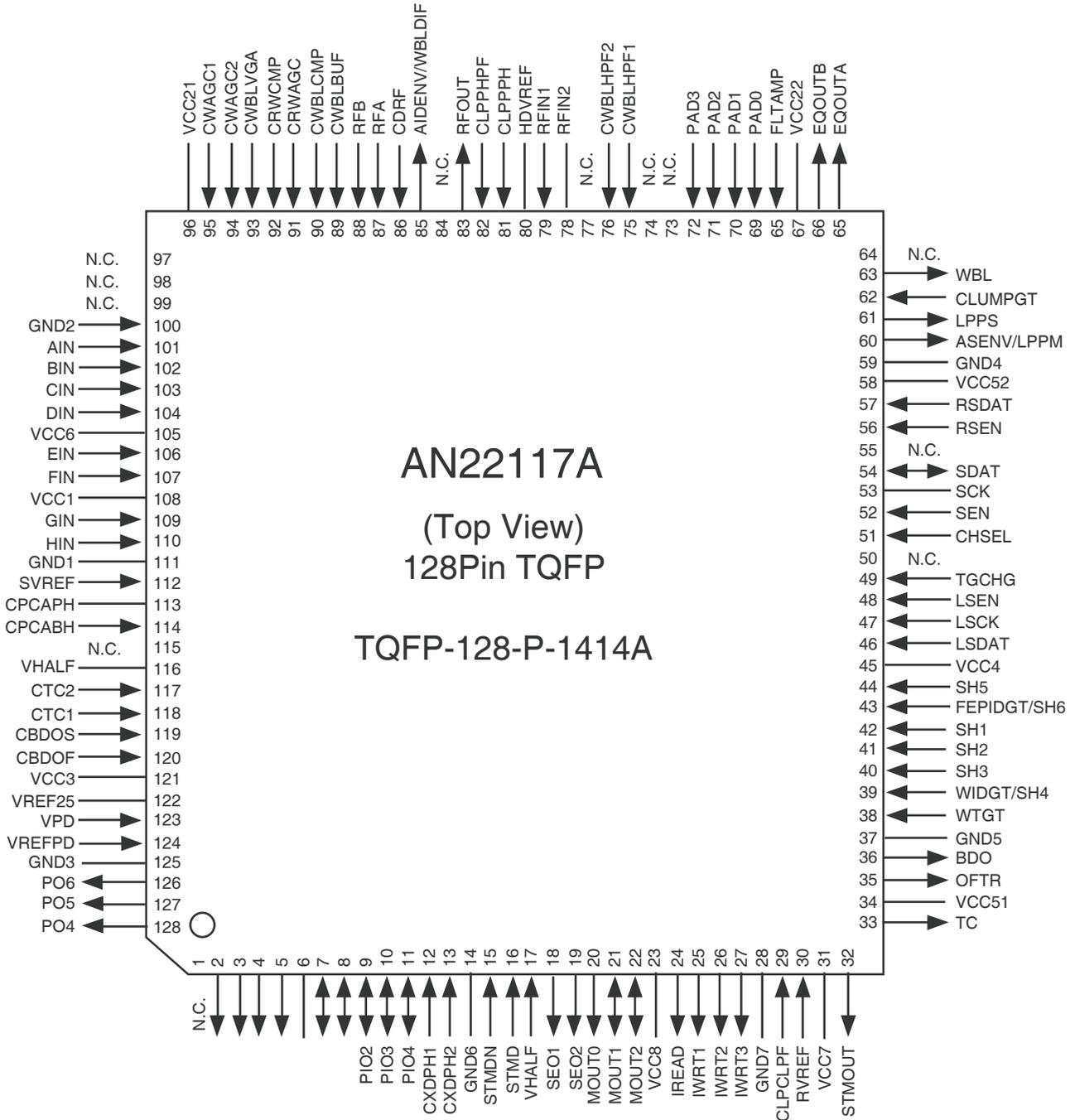
3-1. Spindle Servo Process



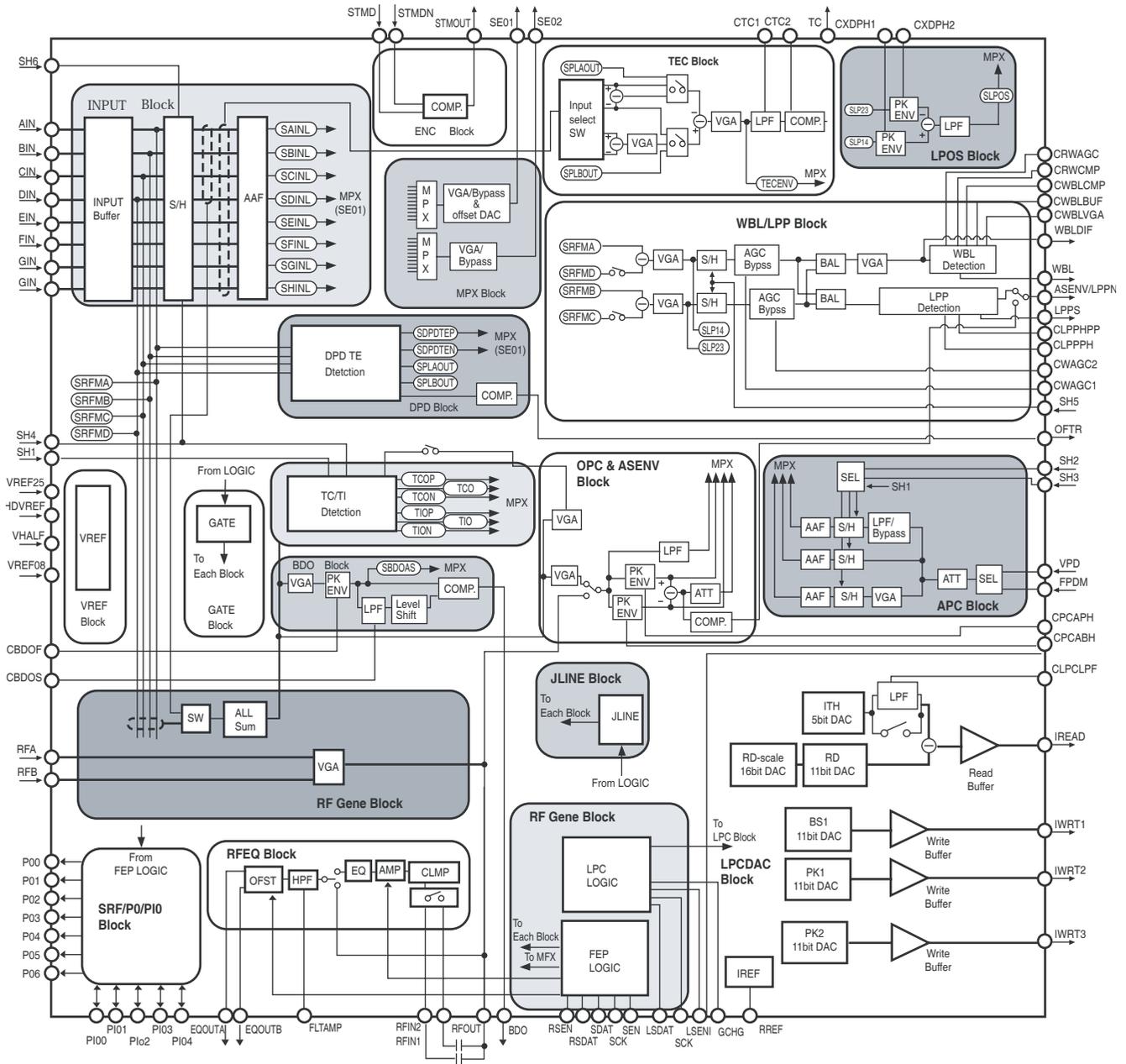
MAJOR IC INTERNAL BLOCK DIAGRAM AND PIN DESCRIPTION

1. LIC101 (AN22117A) : FEP(RF) ANALOG SIGNAL PROCESSOR

- Pin Assignment



• **Block Diagram**



- Pin Assignment

Pin no.	Pin Name	Type	Function
1	NC	-	-
2	PO3	O	General CMOS output pin
3	PO2	O	Head Amp/OEIC gain change signal output pin 3.
4	PO1	O	Head Amp/OEIC gain change signal output pin 2.
5	PO0	O	Head Amp/OEIC gain change signal output pin 1.
6	VCC53	PS	Power supply pin for CMOS I/F & LOGIC.
7	PIO0	I/O	General CMOS Input/Output pin 0.
8	PIO1	I/O	General CMOS Input/Output pin 1.
9	PIO2	I/O	General CMOS Input/Output pin 2.
10	PIO3	I/O	General CMOS Input/Output pin 3.
11	PIO4	I/O	General CMOS Input/Output pin 4.
12	CXDPH1	I	PH capacitor connection pin 1 for LPOS.
13	CXDPH2	I	PH capacitor connection pin 2 for LPOS
14	GND6	PS	GND pin for BG.
15	STMDN	I	PD input pin for STM.
16	STMD	I	PD input pin for STM.
17	VREF08	O	0.8V reference voltage output pin (APC).
18	SEO1	O	Output pin 1 after selection of each error signal.
19	SEO2	O	Output pin 2 after selection of each error signal.
20	MOUT0	O	Analog monitor 0.
21	MOUT1	I/O	Analog monitor 1.
22	MOUT2	I/O	Analog monitor 2.
23	VCC8	PS	Power supply pin for LPC (5.0V)
24	IREAD	O	DAC electric current output pin for READ.
25	IWRT1	O	DAC electric current output pin 1 for WRITE.
26	IWRT2	O	DAC electric current output pin 2 for WRITE.
27	IWRT3	O	DAC electric current output pin 3 for WRITE.
28	GND7	PS	GND pin for LPC.
29	CLPCLPF	I	Capacitor connection pin for LPC/DAC LPF.
30	RVREF	I	Capacitor connection pin for reference voltage setting.
31	VCC7	PS	Power supply pin for LPC (3.3V).
32	STMOUT	O	Encoder circuit comparator output.
33	TC	O	Track cross signal output.
34	VCC51	PS	Power supply pin for CMOS I/F & LOGIC(3.3V)
35	OFTR	O	OFTR signal output.
36	BDO	O	BDO output.
37	GND5	PS	Ground pin for CMOS I/F.
38	WTGT	I	Write gate signal input pin (pull-down)
39	WIDGT/SH4	I	VFO through signal input pin. ROPC mark detection sampling signal input pin (pull-down)
40	SH3	I	PCA average detection, APC space detection/Playback power detection/ Erase detection sample timing signal input pin(pulldown).

Pin no.	Pin Name	Type	Function
41	SH2	I	PCA peak/bottom detection, APC space detection/ Playback power detection/Erase detection sample timing signal input pin (pulldown)
42	SH1	I	ROPC space detection, APC space detection/ Playback power detection sample timing signal input pin(pulldown).
43	FEPIDGT/SH6	I	CAPA through signal input pin/servo sampling signal input pin (pull-down)
44	SH5	I	Sample-and-hold timing signal input pin of wobble S/H at recording (pull-down)
45	VCC4	PS	Power supply pin for internal LOGIC (5.0V)
46	LSDAT	I/O	Serial data input for LPC.
47	LSCK	I	Serial clock enable input LPC.
48	LSEN	I	Serial enable input for LPC.
49	TGCHG	I	LPC DAC bank change control signal input pin.
50	NC	-	-
51	CHSEL	I	Serial MPX channel change data input pin.
52	SEN	I	Serial enable input pin for FEP (pull-down)
53	SCK	I	Serial clock input pin for FEP (pull-up).
54	SDAT	I/O	Serial data input pin for FEP.
55	NC	-	-
56	RSEN	I	Serial enable input for RF (pull-down).
57	RSDAT	I	Serial signal data input for RF
58	VCC52	PS	Power supply pin for CMOS I/F & internal current source power supply pin2 (3.3V)
59	GND4	PS	Ground pin for internal LOGIC
60	ASENV/LPPM	O	ASENV output/LPP mark output pin
61	LPPS	O	LPP space output pin
62	CLUMPGT	I	RFAGC input bias circuit clamp setting input pin (pulldown)
63	WBL	O	WBL binary output
64	NC	-	-
65	EQOUTA	O	Equalizer filter output pin 1.
66	EQOUTB	O	Equalizer filter output pin 2.
67	VCC22	PS	Power supply pin for RFEQ/LPP (5.0V)
68	FLTAMP	I	Filter final stage AMP reference voltage stabilization pin.
69	PAD0	I	A/D input pin 0
70	PAD1	I	A/D input pin 1
71	PAD2	I	A/D input pin 2
72	PAD3	I	A/D input pin 3
73	NC	-	-
74	NC-	-	-
75	CWBLHPF1	I	HPF capacitor connection pin for WBLAGC 1.
76	CWBLHPF2	I	HPF capacitor connection pin for WBLAGC 2.
77	NC	-	-

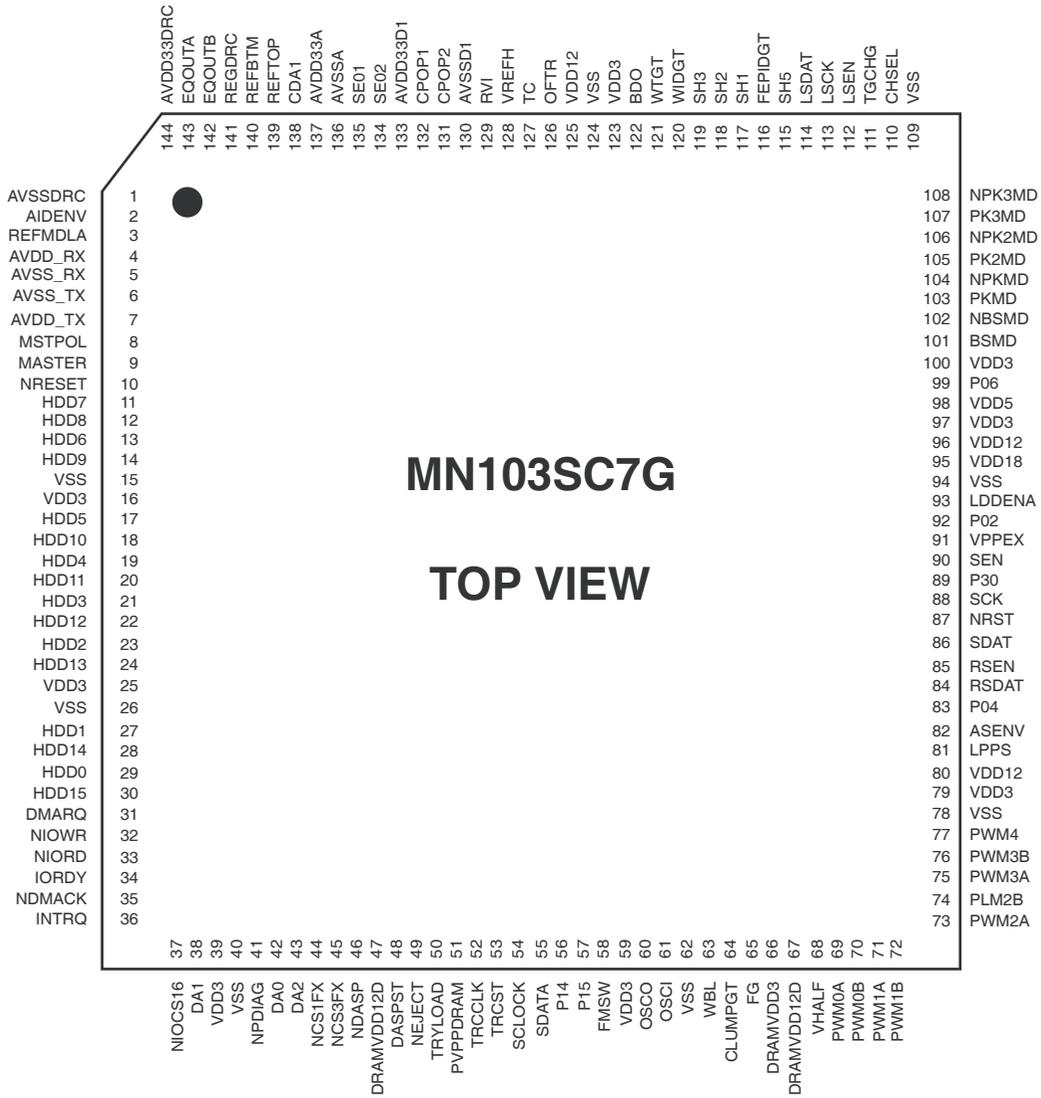
Pin no.	Pin Name	Type	Function
78	RFIN2	I	RFAGC signal input pin 2.
79	RFIN1	I	RFAGC signal input pin 1.
80	HDVREF	O	2.2V reference voltage output pin.
81	CLPPPH	I	Capacitor connection pin for LPP peak hold
82	CLPPHPF	I	Capacitor connection pin for LPPHPF
83	RFOUT	O	RF signal output pin.
84	NC	-	-
85	AIDENV/WBLDIF	O	ASENV binary output/Differential signal output pin for ADIP detection
86	CDRF	I	CD RF signal input pin.
87	RFA	I	DVD RF differential input pin 1.
88	RFB	I	DVD RF differential input pin 2.
89	CWBLBUF	I	Capacitor connection pin for WBLDIF.
90	CWBLCMP	I	Floating Capacitor connection pin for VGA before WBL binary.
91	CRWAGC	I	AGC adjustment capacitor connection pin for +RW.
92	CRWCMP	I	Floating Capacitor connection pin for VGA before WBLDIF AGC.
93	CWBLVGA2	I	Floating Capacitor connection pin for VGA before SRL.
94	CWAGC2	I	AGC adjustment capacitor connection pin 2 for WBL extraction.
95	CWAGC1	I	AGC adjustment capacitor connection pin 1 for WBL extraction.
96	VCC21	PS	-
97	NC	-	-
98	NC	-	-
99	NC	-	-
100	GND2	PS	Power supply pin for RF gene/WBL (5.0V)
101	AIN	I	DVD Tracking input pin 1.
102	BIN	I	DVD Tracking input pin 2.
103	CIN	I	DVD Tracking input pin 3.
104	DIN	I	DVD Tracking input pin 4.
105	VCC6	PS	Power supply pin for DPD (3.3V)
106	EIN	I	CD main signal input pin 1.
107	FIN	I	CD main signal input pin 2.
108	VCC1	PS	Power supply pin for INPUT MATRIX/SERVO (5.0V)
109	GIN	I	CD servo signal input pin 1.
110	HIN	I	CD servo signal input pin 2.
111	GND1	PS	Ground pin for INPUT MATRIX/SERVO/DPD.
112	SVREF	I	OEIC signal reference level input pin.
113	CPCAPH	I	PCA pick hold capacitor connection pin.
114	CPCABH	I	PCA bottom bold capacitor connection pin.
115	NC	I	-
116	VHALF	O	Reference voltage output pin 1/2 VCC (3.3V).
117	CTC2	I	Floating capacitor connection pin for tracking error binary.

Pin no.	Pin Name	Type	Function
118	CTC1	I	Capacitor connection pin for TC HPF.
119	CBDOS	I	Capacitor connection pin for BDO detecting circuit LPF.
120	CBDOF	I	Capacitor connection pin for BDO detecting circuit Pick detection.
121	VCC3	PS	Power supply pin for APC/OPC/ASENV (5.0V).
122	VREF25	O	2.5V reference voltage output pin.
123	VPD	I	DVD front monitor signal input pin.
124	VREFPD	I	Front light system reference level input pin.
125	GND3	PS	Ground pin for APC/OPC/ASENV.
126	PO6	O	Ground CMOS output pin 6.
127	PO5	O	Ground CMOS output pin 5.
128	PO4	O	Ground CMOS output pin 4.

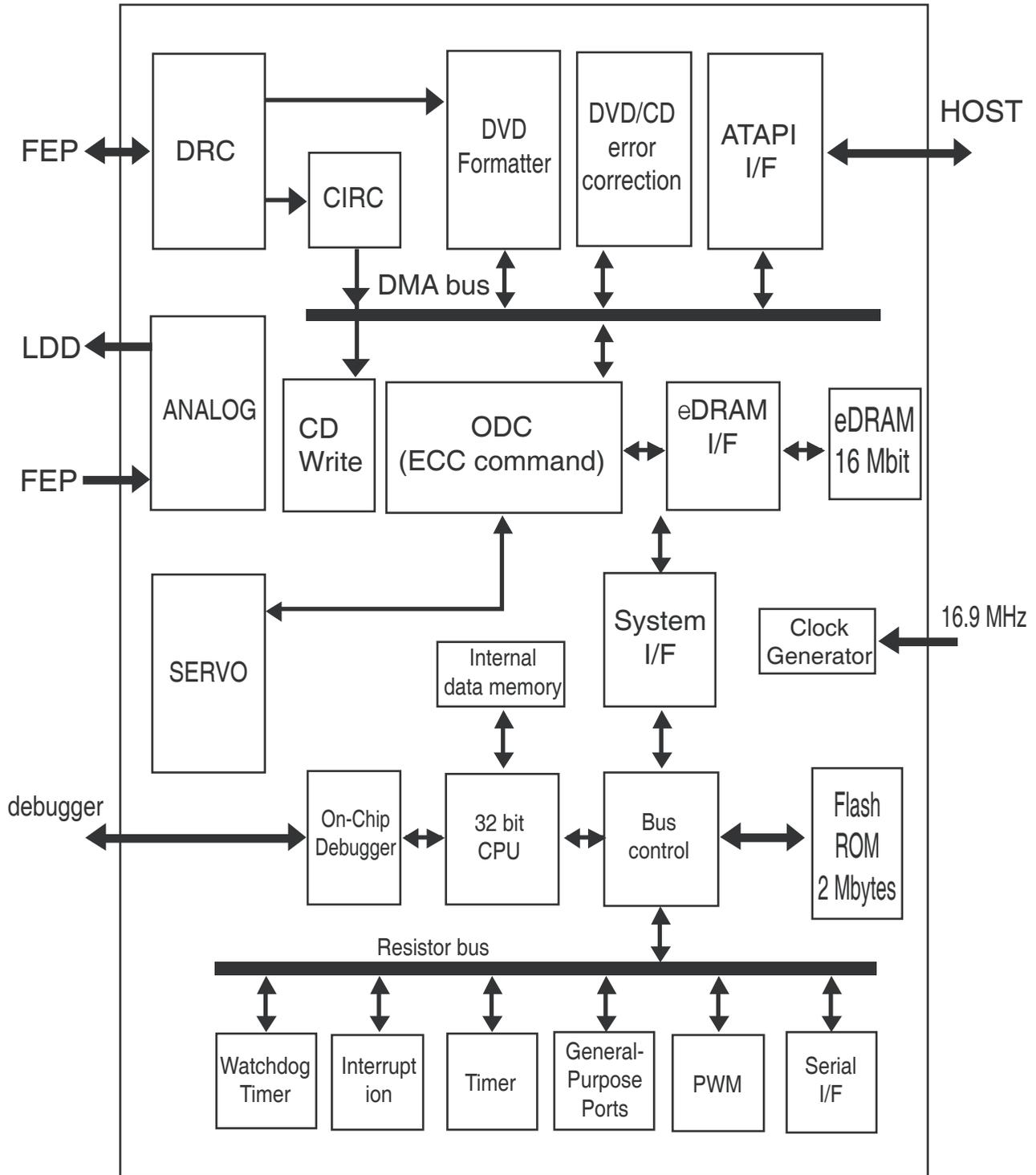
I : Input pin O : Output pin I/O : I/O pin PS : Power supply/Ground pin N.C: Non Connection

2. LIC201 (MN103SC7G) : ENCODER, DECODER & DSP SINGAL PROCESSOR

- Pin Assignment



- Block Diagram (SODC : MN103SC7G)



- Pin Table

Pin Number	Pin Name	I/O	Connection Target	Description
1	AVSSDRC	GND	GND	DRC analog Vss
2	AIDENV	I	FEP	TE signal for DVD-RAM
	WBLDIF			ADIP detector signal input
3	REFMDLA	O	Cap	Analog-to-digital converter reference voltage for ADIP
4	AVDD_RX	Power supply	Power supply	Analog power supply (3.3V)
5	AVSS_RX	GND	GND	Analog ground
6	AVSS_TX	GND	GND	Analog ground
7	AVDD_TX	Power supply	Power supply	Analog power supply (3.3V)
8	MSTPOL	I/O	-	MASTER pin polarity switch
	TRCDATA 1		-	Trace data 1
	P17		-	General-purpose I/O (GIO/PWM1)
9	MASTER	I/O	HOST	ATAPI master/slave signal
	P23		-	General-purpose I/O (GIO/TxD0/PWM0)
10	NRESET	I	HOST	ATAPI reset signal
11	HDD7	I/O	HOST	ATAPI data I/O
12	HDD8	I/O	HOST	ATAPI data I/O
13	HDD6	I/O	HOST	ATAPI data I/O
14	HDD9	I/O	HOST	ATAPI data I/O
15	VSS	GND	GND	Digital Vss
16	VDD3	Power supply	Power supply	I/O pad VDD (3.3V)
17	HDD5	I/O	HOST	ATAPI data I/O
18	HDD10	I/O	HOST	ATAPI data I/O
19	HDD4	I/O	HOST	ATAPI data I/O
20	HDD11	I/O	HOST	ATAPI data I/O
21	HDD3	I/O	HOST	ATAPI data I/O
22	HDD12	I/O	HOST	ATAPI data I/O
23	HDD2	I/O	HOST	ATAPI data I/O
24	HDD13	I/O	HOST	ATAPI data I/O
25	VDD3	Power supply	Power supply	I/O pad VDD (3.3V)
26	VSS	GND	GND	Digital Vss
27	HDD1	I/O	HOST	ATAPI data I/O
28	HDD14	I/O	HOST	ATAPI data I/O
29	HDD0	I/O	HOST	ATAPI data I/O
30	HDD15	I/O	HOST	ATAPI data I/O
31	DMARQ	O	HOST	DMA request to ATAPI host
32	NIOWR	I/O	HOST	ATAPI host write signal
33	NIORD	I/O	HOST	ATAPI host read signal
34	IORDY	O	HOST	Ready signal to ATAPI host
35	NDMACK	I	HOST	ATAPI host DMA acknowledge signal

Pin Number	Pin Name	I/O	Connection Target	Description
36	INTRQ	O	HOST	ATAPI Interrupt request to ATAPI host
37	NIOCS16	I/O	HOST	ATAPI host bus width select signal
	P22		-	General-purpose I/O (GIO)
38	DA1	I	HOST	ATAPI host address signal input
39	VDD3	Power supply	Power supply	I/O pad VDD (3.3V)
40	VSS	GND	GND	Digital Vss
41	NPDIAG	I/O	HOST	Diagnostic signal from ATAPI slave to master
42	DA0	I	HOST	ATAPI host address signal
43	DA2	I	HOST	ATAPI host address signal
44	NCS1FX	I	HOST	ATAPI host chip select signal
45	NCS3FX	I	HOST	ATAPI host chip select signal
46	NDASP	I/O	HOST	ATAPI host chip select signal
47	DRAMVDD12D	Power supply	Power supply	DRAM VDD (1.2V)
48	DASPST	I/O	-	DASP setting
	TRCDATA0		-	Trace data 0
	P16		-	General-purpose I/O (GIO/PWM0)
49	NEJECT	I/O	Mecha	Tray eject signal (SODC external interrupt)
	P25		-	General-purpose I/O (GIO)
50	TRYLOAD	I/O	Mecha	Tray eject signal (SODC external interrupt)
	P26		-	General-purpose I/O (GIO)
51	PVPPDRAM	Power supply	Cap	DRAM internal power supply output
52	TRCCLK	I/O	-	Trace clock
	P20		-	General-purpose I/O (GIO/TxD0/PWM0)
53	TRCST	I/O	-	Trace status
	P21		-	General-purpose I/O (GIO/RxT0/PWM1)
54	SCLOCK	I/O	-	Debugger clock
55	SDATA	I/O	-	Debugger data
56	P14	I/O	-	General-purpose I/O(GIO/SerialCLK0/PWM0/external interrupt 3)
	TRCDATA2		-	Trace data 2
	EXTRIG1		-	Trigger 1
57	P15	I/O	-	General-purpose I/O(GIO/RxD0/PWM1/external interrupt 4)
	TRCDATA3		-	Trace data 3
	EXTRIG2		-	Trigger 2
58	FMSW	I/O	PU	Power monitor detector multiplier conversion signal
	P03		-	General-purpose I/O (GIO)
60	OSCO	O	X'tal	Oscillator output
61	OSCI	U	X'tal	Oscillator input (16.9344 MHz)
62	VSS	GND	GND	Digital Vss
63	WBL	I	FEP	Wobble binary signal

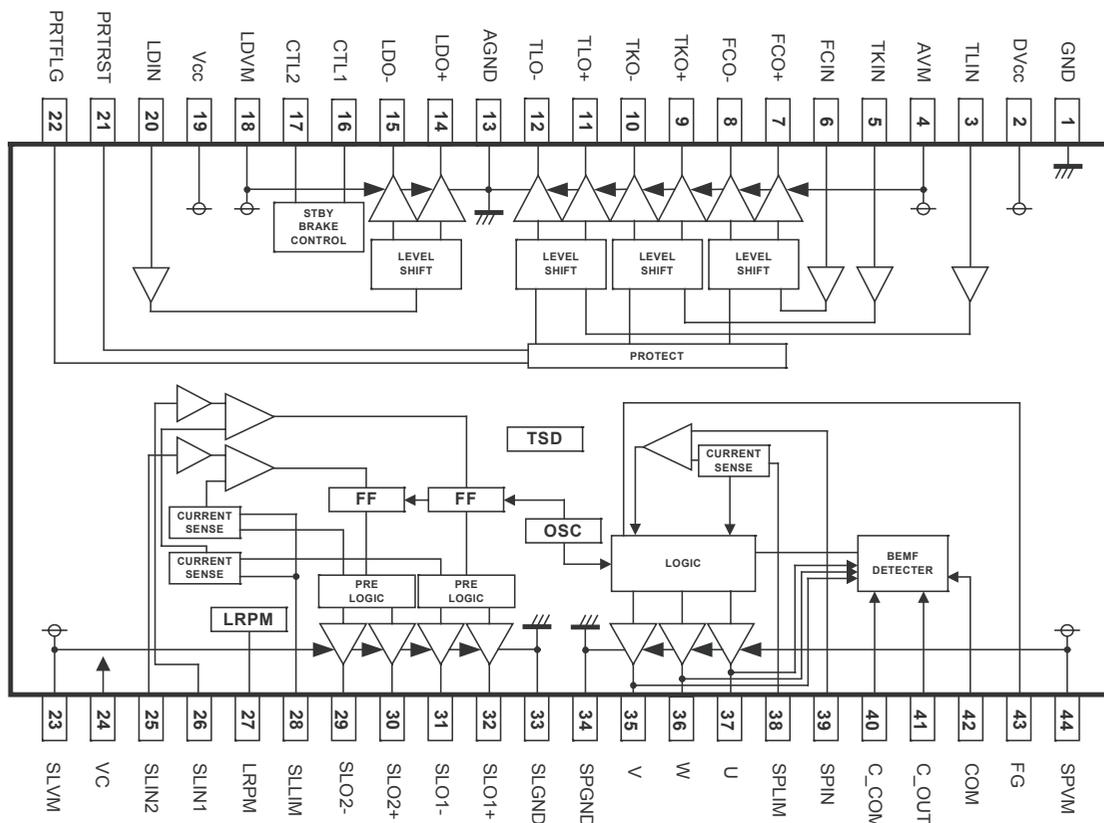
Pin Number	Pin Name	I/O	Connection Target	Description
64	CLUMPGT	O	FEP	RF AGC bias circuit clamp signal
65	FG	I	DRIVER	Spindle FG input
66	DRAMVDD3	Power supply	Power supply	DRAM VDD (3.3V)
67	DRAMVDD12D	Power supply	Power supply	DRAM VDD (1.2V)
68	VHALF	I/O	FEP	Drive pin central reference voltage input
69	PWM0A	O	DRIVER	Focus drive differential PWM+ output, focus drive BSDA output.
70	PWM0B	I/O	DRIVER	Focus drive differential PWM- output
	P10		-	General-purpose I/O (GIO/TxD0/SerialCLK0/PMW0)
71	PWM1A	O	DRIVER	Focus 2 (tilt) drive differential PWM+ output, focus 2 drive BSDA output.
72	PWM1B	I/O	DRIVER	Focus 3 (tilt) drive differential PWM-output
	P11		-	General-purpose I/O (GIO/RxD0/PWM1)
73	PWM2A	I/O	DRIVER	Tracking drive differential PWM+ output, tracking drive BSDA output
	P27		-	General-purpose I/O (GIO/PWM0)
74	PWM2B	I/O	DRIVER	Tracking drive differential PWM - output
	TX		HOST	IEC60958-compliant digital output
	P12		-	General-purpose I/O (GIO/TxD0)
75	PWM3A	I/O	DRIVER	Traverse drive differential PWM+ output, stepper 1 drive output
	P31		-	General-purpose I/O (GIO/PWM0)
76	PWM3B	I/O	DRIVER	Traverse drive differential PWM- output, stepper 2 drive output
	P31		-	General-purpose I/O (GIO/RxD0/PWM1)
77	PWM4	O	DRIVER	Spindle drive output
78	VSS	GND	GND	Digital Vss
79	VDD3	Power supply	Power supply	I/O pad VDD (3.3V)
80	VDD12	Power supply	Power supply	Internal logic VDD(1.2V)
81	LPPS	I	FEP	LPP space input
82	ASENV	I	FEP	ASENV input
	LPPM			LPP mark input
83	P04	I/O	-	General-purpose I/O (GIO/TxD0/PWM1/external interrupt 1)
	GENE0		Mache	Inner limit switch input
84	RSDAT	I/O	FEP	FEP serial interface data 2 (RF)
85	RSEN	O	FEP	FEP serial interface enable 2 (RF)
86	SDAT	I/O	FEP	FEP serial interface data
87	NRST	I	Reset	IC Reset input (power on reset)
88	VDD3	Power supply	Power supply	I/O pad VDD(3.3)
89	P30	I/O	-	General-purpose I/O (GIO/TxD1)
90	SEN	O	FEP	FEP serial interface enable

Pin Number	Pin Name	I/O	Connection Target	Description
91	VPPEX	Power supply	Power supply	Flash memory power supply Vpp
92	P02	I/O	-	General-purpose I/O (GIO/RxD0/PWM0/external interrupt 0)
	NLDERR		PU	Laser error detection signal
93	LDDENA	O	PU	LDD enable signal
94	VSS	GND	GND	Digital Vss
95	VDD18	Power supply	Power supply	Flash memory power supply Vpp
96	VDD12	Power supply	Power supply	Internal logic VDD (1.2V)
97	VDD3	Power supply	Power supply	I/O pad VDD (1.2V)
98	VDD5	Power supply	Power supply	DRAM VDD (5.0V)
99	P06	I/O	-	General-purpose I/O (GIO/RxD0/PWM1/external interrupt 2)
	HFON		PU	External high frequency module (HFM) ON/OFF
100	VDD3	Power supply	Power supply	I/O pad VDD (1.2V)
101	BSMD	O	PU	BIAS modulation signal differential current output
102	NBSMD	O	PU	NBIAS modulation signal differential current output
103	PKMD	O	PU	PEAK1 modulation signal differential current output
104	NPKMD	O	PU	NPEAK1 modulation signal differential current output
105	PK2MD	O	PU	PEAK2 modulation signal differential current output
106	NPK2MD	O	PU	NPEAK2 modulation signal differential current output
107	PK3MD	I/O	PU	PEAK3 modulation signal differential current output
	SRF1			OEIC gain switching timing adjustment 1 (when using external WTST)
	P00			General-purpose I/O (GIO/TxD0/PWM0)
108	NPK3MD	I/O	PU	NPEAK3 modulation signal differential current output
	SRF2			OEIC gain switching timing adjustment 2 (when using external WTST)
	P01			General-purpose I/O (GIO/RxD0/PWM1)
109	VSS	GND	GND	Digital Vss
110	CHSEL	I/O	FEP	Serial MPX channel conversion data output signal
	MMOD		-	Test mode selection signal(Do not connect to a pull-up resistor or similar part.)
111	TGCHG	I/O	FEP	Write power switch signal
	P05		-	General-purpose I/O (GIO)
112	LSEN	O	PU	LDD serial interface enable
113	LCK	O	PU	LDD serial interface clock
114	LSDAT	I/O	PU	LDD serial interface data
115	SH5	I/O	FEP	Write WOBBLE sample and hold sampling signal
116	FEPIDGT	I/O	FEP	CAPA punch out signal
	SH6			Servo S/H sample signal
	P07		-	General-purpose I/O (GIO/Serial CLK1)

Pin Number	Pin Name	I/O	Connection Target	Description
117	SH1	I/O	FEP	Sample timing signal for ROPC space detection, APC space detection, and read power detection
118	SH2	I/O	FEP	Sample timing signal for PCA peak, bottom detection, APC peak detection, and mean valuer detection
119	SH3	I/O	FEP	Sample timing signal for PCA mean value detection, APC space detection, and read power detection, and erase detection
120	WIDGT	I/O	FEP	VFO punch out signal
	SH4			ROPC mark detection sampling signal
	P24		-	General-purpose I/O (GIO/TxD1)
121	WTGT	O	FEP	Write gate
122	BDO	I	FEP	Dropout signal input
123	VDD3	Power supply	Power supply	I/O pad VDD (3.3V)
124	VSS	GND	GND	Digital Vss
125	VDD12	Power supply	Power supply	Internal logic VDD (1.2V)
126	OFTR	I	FEP	Off track signal input
127	TC	I	FEP	Track crossing signal input
128	VREFH	I	FEP	2.2V reference voltage input
129	RVI	I/O	Res.	Fixed current source for LVDS, WBL, and analog blocks
130	AVSSD1	GND	GND	WOBBLE analog Vss
131	CPOP2	I/O	Cap. Res.	Filter connection pin for wobble PLL
132	CPOP1	I/O	Cap. Res.	Filter connection pin for wobble PLL
133	AVDD33DI	Power supply	Power supply	WOBBLE analog VDD (3.3V)
134	SE02	I	FEP	Error signal output after selection, analog input
135	SE01	I	FEP E	rror signal output after selection, analog input
136	AVSSA	GND	GND	Servo analog-to-digital converter analog Vss
137	AVDD33A	Power supply	Power supply	Servo analog-to-digital converter analog VDD (3.3V)
138	CDA1	O	Cap	Smoothing capacitance for DRC-VCO
139	REFTOP	O	Cap	Analog-to-digital converter reference voltage for DRC (TOP)
140	REFBTM	O	Cap	Analog-to-digital converter reference voltage for DRC (BOTTOM)
141	REGDRC	O	Cap	DRC analog-to-digital converter analog VDD (1.2V) Internal regurator output
142	EQOUTB	I	FEP	RF differential signal (NEG)
143	EQOUTA	I	FEP	RF differential signal (POS)
144	AVDD33DRC	Power supply	Power supply	DRC analog-to-digital converter analog VDD (3.3 V)

3. LIC301 (BD7776ARFS) : CD-ROM/DVD-ROM 7CH POWER DRIVER

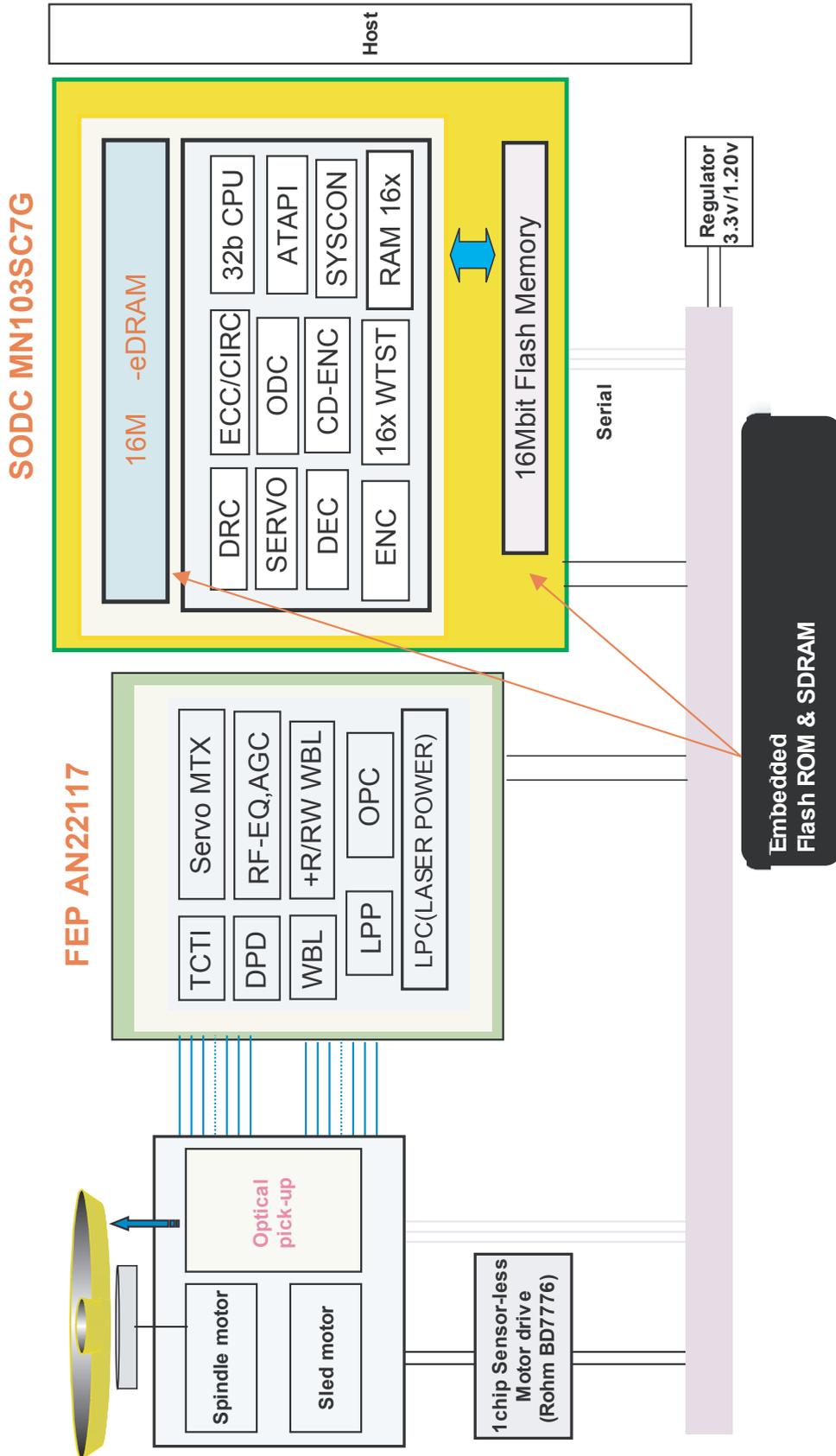
- Block Diagram



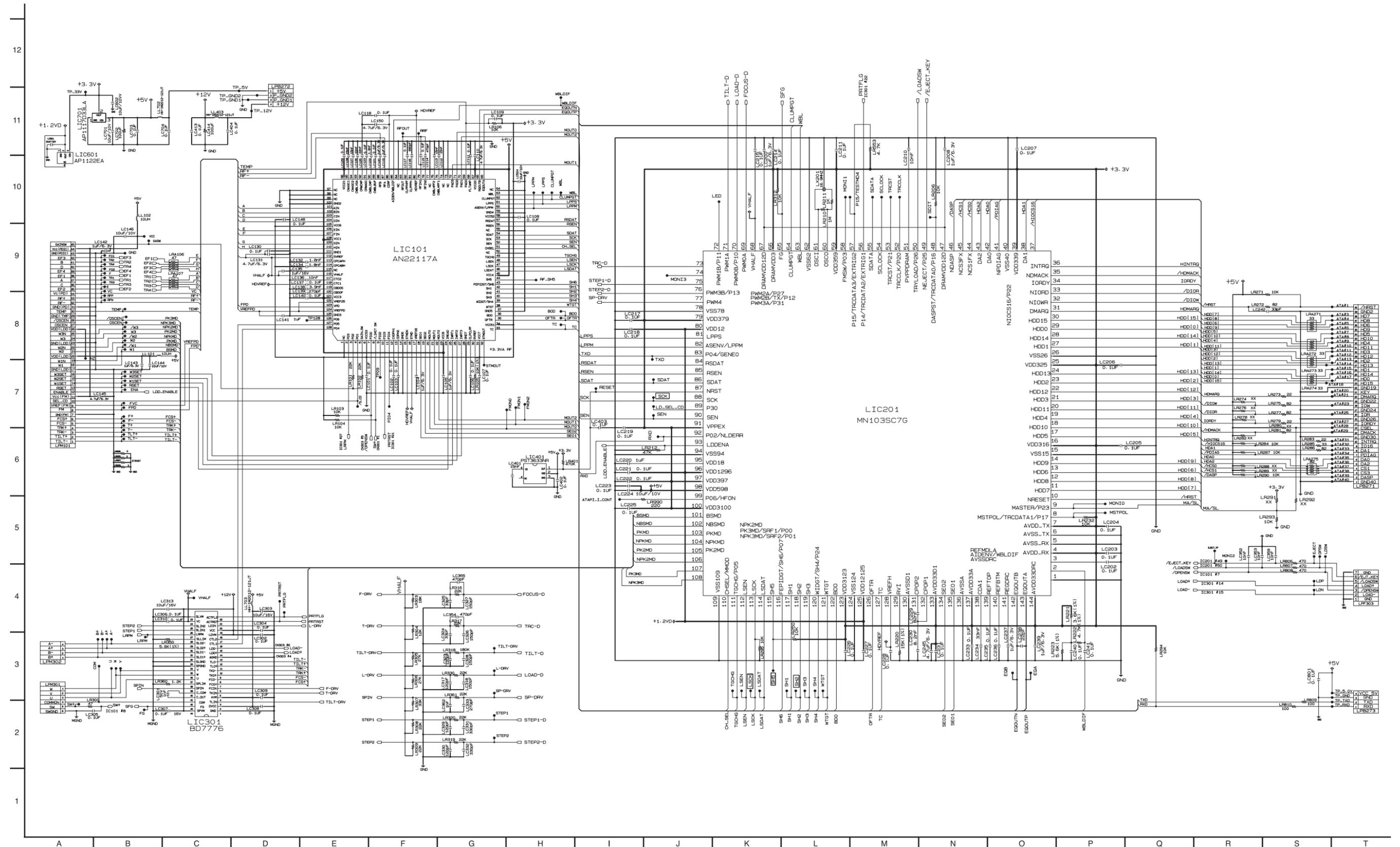
- Pin Function

No	Pin name	Description	No	Pin name	Description
1	GND	GND	23	SLVM	Motor driver power supply
2	DVcc	PWM block control power supply	24	VC	Reference voltage input
3	TLIN	Tilt motor driver input	25	SLIN2	Motor driver input2
4	AVM	Actuator driver block power supply	26	SLIN1	Motor driver input1
5	TKIN	Tracking driver input	27	LRPM	Low speed rotational motor transfer terminal
6	FCIN	Focus driver input	28	SLLIM	Input terminal for slide current limit
7	FCO+	Focus driver inverted output	29	SLO2-	Motor driver 2 non-inverted output
8	FCO-	Focus driver non-inverted output	30	SLO2+	Motor driver 2 inverted output
9	TKO+	Tilt driver inverted output	31	SLO1-	Motor driver 1 non-inverted output
10	TKO-	Tilt driver non-inverted output	32	SLO1+	Motor driver 1 inverted output
11	TLO+	Tracking driver inverted output	33	SLGND	Motor driver power supply GND
12	TLO-	Tracking driver non-inverted output	34	SPGND	Spindle driver power supply GND
13	AGND	BTL driver GND	35	V	Spindle driver output V
14	LDO+	Loading driver inverted output	36	W	Spindle driver output W
15	LDO-	Loading driver non-inverted output	37	U	Spindle driver output U
16	CTL1	Loading driver control input	38	SPLIM	Input terminal for spindle current limit
17	CTL2	Loading driver control input	39	SPIN	Spindle control voltage input
18	LDVM	Loading driver power supply	40	C_COM	Condenser connection terminal (com)
19	Vcc	Power supply	41	C_OUT	Condenser connection terminal (OUT)
20	LDIN	Loading driver input	42	COM	Motor coil input terminal
21	PRTTRST	Protect input	43	FG	FG signal output
22	PRTFLG	Protect flag output	44	SPVM	Spindle driver Power supply

BLOCK DIAGRAM



CIRCUIT DIAGRAM



CIRCUIT VOLTAGE CHART

PIN NO.	VOLTAGE
LIC101	
1	3.32
2	0.00
3	0.00
4	0.00
5	0.00
6	3.32
7	0.00
8	3.21
9	3.32
10	0.00
11	0.00
12	3.32
13	3.51
14	0.00
15	2.22
16	1.67
17	0.82
18	2.09
19	1.60
20	0.85
21	0.82
22	0.65
23	4.97
24	0.00
25	0.00
26	0.00
27	0.00
28	0.00
29	0.00
30	1.00
31	3.32
32	0.00
33	3.32
34	3.32
35	0.00
36	0.00
37	0.00
38	0.00
39	0.00
40	0.00
41	0.00
42	0.00
43	0.00
44	0
45	4.97
46	pulse
47	pulse
48	pulse
49	3.31
50	0.00
51	pulse
52	pulse

PIN NO.	VOLTAGE
53	pulse
54	pulse
55	0.00
56	pulse
57	pulse
58	3.32
59	0.00
60	3.32
61	3.32
62	0.00
63	0.00
64	0.00
65	2.04
66	2.04
67	4.97
68	2.21
69	1.20
70	0.65
71	0.85
72	0.82
73	0.00
74	0.00
75	0.00
76	0.00
77	0.00
78	0.00
79	2.18
80	2.22
81	0.00
82	2.20
83	2.22
84	0.00
85	0.00
86	2.22
87	2.18
88	2.18
89	0.00
90	2.23
91	1.62
92	1.58
93	1.59
94	0.00
95	0.00
96	4.97
97	0.00
98	0.00
99	0.00
100	0.00
101	1.80
102	1.78
103	1.77
104	1.80
105	3.32

PIN NO.	VOLTAGE
106	1.76
107	1.73
108	4.97
109	1.74
110	1.75
111	0.00
112	1.67
113	0.00
114	0.00
115	0.00
116	1.67
117	2.28
118	2.21
119	3.08
120	4.10
121	4.97
122	2.51
123	2.49
124	2.51
125	0.00
126	0.00
127	3.28
128	3.28
LIC201	
1	0.00
2	2.00
3	3.31
4	3.31
5	0.00
6	0.00
7	3.31
8	3.30
9	0.00
10	3.30
11	pulse
12	pulse
13	pulse
14	pulse
15	0.00
16	3.29
17	pulse
18	pulse
19	pulse
20	pulse
21	pulse
22	pulse
23	pulse
24	pulse
25	3.28
26	0.00
27	pulse
28	pulse
29	pulse

PIN NO.	VOLTAGE
30	pulse
31	pulse
32	pulse
33	pulse
34	pulse
35	pulse
36	pulse
37	4.94
38	3.27
39	3.28
40	0.00
41	4.95
42	3.27
43	3.27
44	pulse
45	3.27
46	4.94
47	1.18
48	0.00
49	3.28
50	0.00
51	2.63
52	0.00
53	0.00
54	3.27
55	3.27
56	0.00
57	3.28
58	0.00
59	3.29
60	OSC
61	OSC
62	0.00
63	0.00
64	0.00
65	pulse
66	3.29
67	1.19
68	1.65
69	1.63
70	1.64
71	1.64
72	0.00
73	1.64
74	0.00
75	1.66
76	1.97
77	1.85
78	0.00
79	3.29
80	1.20
81	3.33
82	3.33

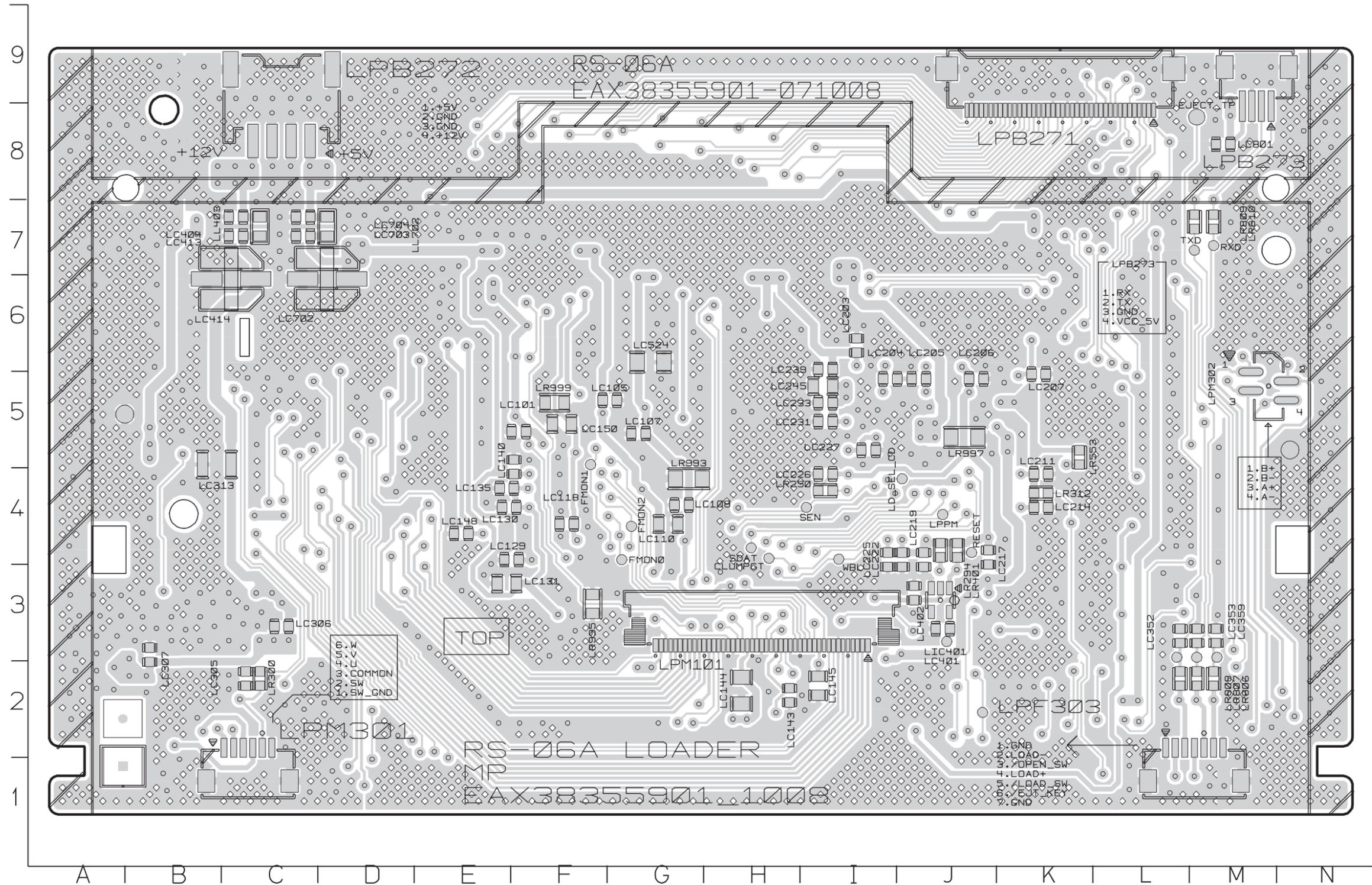
PIN NO.	VOLTAGE
83	3.33
84	pulse
85	pulse
86	pulse
87	3.17
88	pulse
89	0.00
90	pulse
91	3.33
92	3.32
93	3.32
94	0.00
95	1.80
96	1.19
97	3.27
98	4.94
99	3.30
100	3.28
101	1.39
102	1.00
103	1.39
104	1.00
105	1.39
106	0.98
107	1.00
108	1.40
109	0.00
110	pulse
111	3.31
112	pulse
113	pulse
114	pulse
115	3.31
116	0.00
117	0.00
118	0.00
119	0.00
120	0.00
121	0.00
122	0.00
123	3.28
124	0.00
125	1.19
126	0.00
127	3.28
128	2.21
129	1.50
130	0.00
131	0.00
132	0.00
133	3.31
134	1.60
135	2.08

PIN NO.	VOLTAGE
136	0.00
137	3.31
138	0.83
139	2.27
140	1.76
141	1.26
142	2.00
143	2.00
144	3.30
LIC301	
1	0.00
2	4.88
3	1.65
4	4.88
5	1.65
6	1.65
7	2.45
8	2.54
9	2.45
10	2.54
11	2.48
12	2.49
13	0.00
14	6.00
15	6.00
16	3.26
17	3.26
18	12.50
19	12.50
20	1.65
21	0.00
22	0.00
23	12.50
24	1.66
25	1.70
26	1.71
27	0.00
28	1.17
29	12.50
30	12.50
31	12.50
32	12.50
33	0.00
34	0.00
35	PULSE
36	PULSE
37	PULSE
38	1.12
39	1.76
40	PULSE
41	PULSE
42	PULSE
43	PULSE

PIN NO.	VOLTAGE
LIC601	
1.GND	0.00
2.VOUT	1.20
3.VIN	3.30
LIC701	
1.GND	0.00
2.VOUT	3.30
3.VIN	4.95

PRINTED CIRCUIT BOARD DIAGRAMS

1. MAIN P.C.BOARD (TOP VIEW)



2. MAIN P.C.BOARD (BOTTOM VIEW)

